Modularized Equalization Architecture with Voltage Multiplier-Based Cell Equalizer and Switchless Switched Capacitor Converter-Based Module Equalizer for Series-Connected Electric Double-Layer Capacitors

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***Abstract*—This paper proposes a novel modular equalization architecture for series-connected electric double-layer capacitor (EDLC) modules, each consisting of multiple cells connected in series. Cell voltages in a module are equalized by an inductive voltage divider (IVD)-voltage multiplier (VM)-based cell equalizer while module voltages are unified by switched capacitor converters (SCCs). Square wave voltages generated at switching nodes of the IVD-VM-based cell equalizers are utilized to drive the SCC-based module equalizers, realizing the switchless topology of SCC-based module equalizers. The required switch count of the proposed system can be halved compared to conventional systems, allowing simplified circuit. An experimental equalization test for three EDLC modules, each consisting of six cells in series, was performed from an initially voltage-imbalanced condition. Module and cell voltages were equalized at different rates, and the equalization performance of the proposed modular equalization system was successfully demonstrated.**

***Index Terms*—Equalization, inductive voltage divider, modular architecture, switched capacitor converter (SCC), voltage multiplier (VM).**

I. Introduction

Applications of energy storage sources, such as lithium-ion batteries and electric double-layer capacitors (EDLCs), are rapidly expanding from small portable electronic devices to large systems including electric vehicles and renewable energy systems. Vigorous research and development efforts in search of better materials for higher energy density and extended service life of energy storage sources are underway, and performance of energy storage cells are steadily improving. However, in order to fully utilize chargeable/dischargeable energy of cells and exploit life performance of cells, the cell voltage imbalance issue that is very likely in relatively large-scale systems needs to be properly precluded.

Cell voltage imbalance issues are known to originate even from a minor mismatch in cell characteristics. In general, multiple cells are connected in series to form a string with an arbitral voltage level in order to meet voltage requirement of systems. Cell voltages in such systems are gradually imbalanced because of nonuniform capacity/capacitance, self-discharge rate, internal impedance, and temperature. Imbalance due to nonuniform temperature is the most cumbersome issue because it influences many other factors and is dependent on system's thermal design. The causal relationship among voltage imbalance, degradation, and mismatch factors is illustrated in Fig. 1.

The voltage imbalance causes serious problems such as increased risks of over-charging/-discharging and decreased chargeable/dischargeable energy. As long as a string voltage as a whole is regulated during operation, cells in the string are charged/discharged in series. Hence, cells with the highest/lowest voltage are over-charged/-discharged during charging/discharging processes, respectively, likely resulting in accelerated aging and increased hazardous risks. The over-charging/-discharging due to the cell voltage imbalance might be prevented by halting charging/discharging when some cells being charged/discharged beyond safely boundaries are detected. However, since most cells in such case are not fully cycled, it naturally leads to the decreased chargeable/dischargeable energy of the string. Hence, cell voltage equalizers that eliminate voltage imbalance are indispensable to ensure years of safe operation and to fully utilize chargeable/dischargeable energy of the string.

A variety of cell voltage equalizers have been proposed and

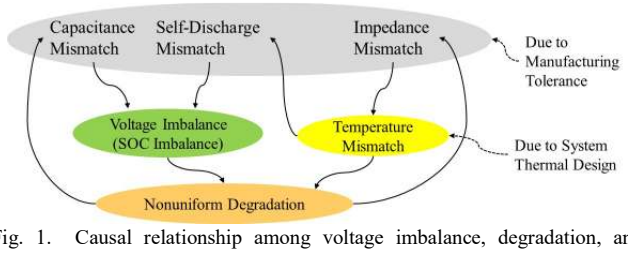

Fig. 1. Causal relationship among voltage imbalance, degradation, and mismatch factors.

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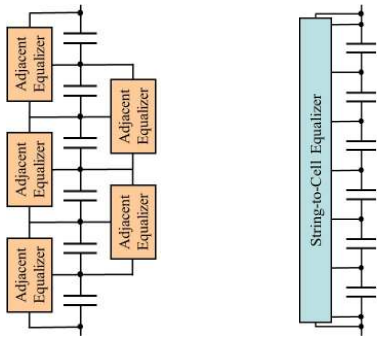


Fig. 2. (a) Adjacent cell-to-cell equalizers and (b) string-to-cell equalizer.

developed [1]. The adjacent cell-to-cell equalization architecture, shown in Fig. 2(a), with which stored energies of cells are transferred only between adjacent cells, are the most straightforward approach. Nonisolated bidirectional converters, such as PWM converters [2]–[6] and switched capacitor converters (SCCs) [7]–[12], are categorized into the adjacent cell-to-cell equalizer. The adjacent cell-to-cell equalizers offer good modularity because the number of cells can be arbitrarily extended with just increasing the number of equalizers. However, the energy storage system is prone to complexity as the number of equalizers, each requiring some switches, is proportional to the number of cells connected in series—for an energy storage system comprising six cells connected in series, for example, five equalizers and ten switches in total are necessary if bidirectional PWM converters each containing two switches are employed.

Meanwhile, the string-to-cell equalization architecture [see Fig. 2(b)], through which energy is transferred from the string to the least charged cell directly, can significantly reduce the numbers of not only equalizers but also switches, achieving simplified system and circuit. A variety of string-to-cell equalizers, such as multi-winding flyback converters [13], multistacked buck-boost converters [14], voltage multipliers [15]–[18], etc. [19]–[23], belong to the string-to-cell equalization architecture. The major drawback of this equalization architecture includes poor modularity—when the number of cells is to be changed due to requirements and applications, string-to-cell equalizers also need to be redesigned with adjusting a turns ratio of a transformer and selecting semiconductor and passive devices with proper voltage ratings.

For large-scale systems, in general, cells are not directly connected in series to form a string. Instead, multiple energy storage modules, each containing several cells, are connected in series to improve the usability and extendibility. A modularized equalization system employing module- and cell-level equalizers [24]–[32] would be a suitable solution to such systems. Modularized equalization systems using an adjacent module-to-module equalizer in conjunction with adjacent cell-to-cell equalizers and module-to-cell equalizers are depicted in Figs. 3(a) and (b), respectively. In modularized systems, two equalizers operate independently and provide different power transfer paths, allowing flexible system design and good modularity by selecting proper equalizer topologies for modules and cells. Different equalizer topologies with different power capabilities can be used as module and cell equalizers. This architecture is considered suitable for relatively large-scale

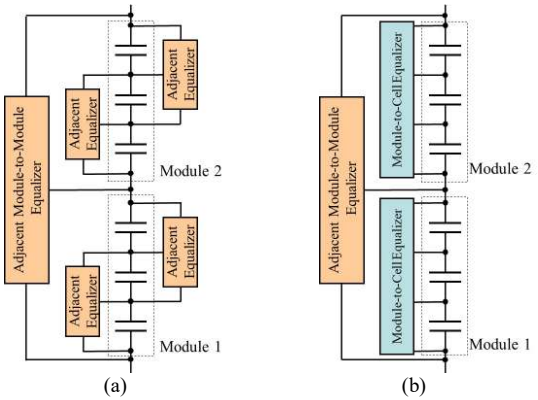


Fig. 3. Modularized equalization architectures using adjacent module-to-module equalizer in conjunction with (a) adjacent cell-to-cell equalizers and (b) module-to-cell equalizer.

systems because different current capabilities would be necessary for module and cell equalizations. Module equalizers should be capable of providing relatively large equalization current to preclude voltage imbalance originating from a relatively large mismatch in module characteristics and temperature—large temperature difference among modules is very likely because of their large volume. Meanwhile, since cell temperatures in a module can be easily evened thanks to their small geometry, equalizers with small currents would suffice for cell equalization.

The modularized architecture shown in Fig. 3(b) is considered advantageous in terms of system design flexibility and circuit simplicity. The string can be flexibly designed by adjusting the number of modules with adjacent module-to-module equalizers while, by fixing the number of cells in each module, a simple module-to-cell equalizer can be employed—adjacent module-to-module equalizers and module-to-cell equalizers offer good modularity and simple circuit, respectively, as mentioned earlier. However, since adjacent module-to-module equalizers still require switches, the system tends to be complex and costly as the number of modules connected in series grows.

To reduce the switch count, a modularized equalization architecture using SCC-based module equalizers and VM-based cell equalizers has been proposed in our prior work [33]. In this paper, the extended and fully developed work about the modular equalization architecture is presented. The rest of this paper is organized as follows. In Section II, key elements as well as the derivation procedure of the proposed modular equalization architecture are explained. In Section III, the overall operation of the modular equalization architecture as a whole is explained, followed by separate analyses for the cell equalizer and switchless module equalizer. Section IV derives a dc equivalent circuit of the modular equalization architecture, and its simulation results are also presented. Experimental results of an EDLC string comprising three modules, each consisting of six cells, will be shown in Section V.

II. Proposed Modular Equalization Architecture

A. Modular Equalization Architecture

The schematic diagram of the proposed equalization architecture is shown in Fig. 4. Although it looks very similar

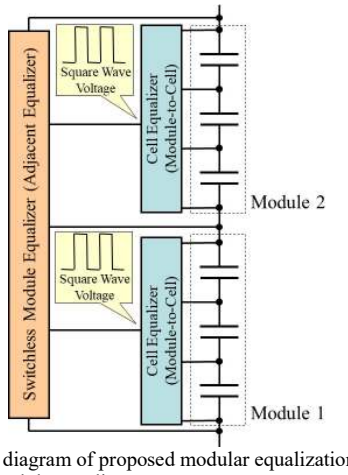


Fig. 4. Schematic diagram of proposed modular equalization on architecture using switchless module equalizers.

to the one shown in Fig. 3(b), the operation principle is totally different. The module- and cell-equalizers in Fig. 3(b) independently operate, whereas those in the proposed system are connected and interdependent; the switchless module equalizer is driven by square wave voltages generated at switching nodes in the cell equalizers, as shown in the insets of Fig. 4. Utilizing these square wave voltages realizes the switchless topology of module equalizers. Details of module and cell equalizers will be discussed in the following subsections.

B. Key Elements for Proposed Modular Equalization Architecture

Similar to the conventional systems shown in Fig. 3(b), the proposed modular system consists of two different types of equalizers. Various kinds of adjacent module-to-module (or cell-to-cell) equalizer topologies, such as the SCC and bidirectional PWM converter, can be used as module equalizers. In this paper, the SCC, shown in Fig. 5(a), is employed because of its simple circuit and operation principle. In the conventional SCC, the odd- and even-numbered switches are alternately driven with a fixed 50% duty cycle in a complementary mode, and square wave voltages appear at switching nodes, as depicted in the insets.

A conventional half-bridge voltage multiplier (HBVM)-based cell equalizer [15] for four cells connected in series is shown in Fig. 5(b). The simple circuit is the most appealing feature of this topology as only two switches are necessary regardless of the number of cells. This equalizer is applicable to any number of cells by adjusting the VM's structure. Although this topology requires a bulky expensive transformer to produce a square wave voltage with an arbitrary peak-to-peak voltage of V_{mod}/N (where V_{mod} and N are the module voltage and transformer turns ratio, respectively), a novel transformerless version will be introduced as a cell equalizer in the proposed system in this work (see next subsection). The high- and low-side switches (Q_H and Q_L) operate with a fixed 50% duty cycle, and the half-bridge inverter generates a square wave voltage to drive the VM that comprises passive elements only. AC voltage/current transferred to the transformer's secondary side is rectified by the VM, and the least charged cell having the lowest voltage in the module preferentially receives an equalization current from the VM. The detailed equalization

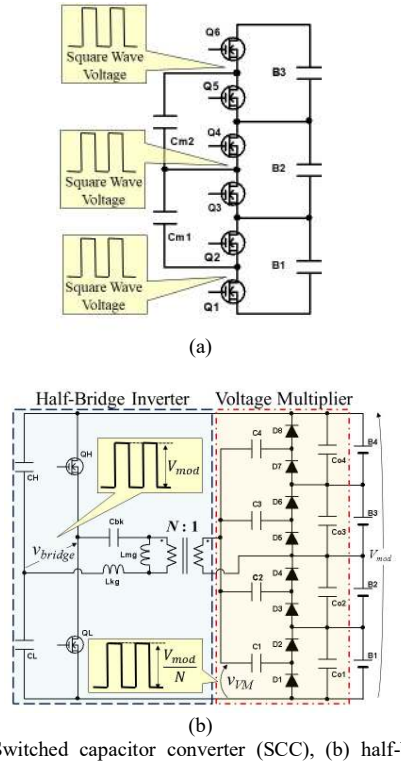


Fig. 5. (a) Switched capacitor converter (SCC), (b) half-bridge voltage multiplier (VM) using transformer.

mechanism by the VM can be found in [15]–[18].

C. Circuit Derivation

By utilizing the square wave voltages generated in the HBVM-based cell equalizers for driving the SCC-based module equalizers, switches in module equalizers can be eliminated, realizing the switchless module equalizers. The derived modular equalization system using inductive voltage divider-VM (IVD-VM)-based cell equalizers and switchless SCC-based module equalizers for three modules is shown in Fig. 6, as an example. An equivalent series resistance (ESR) R_m and equivalent series inductance (ESL) L_m of the capacitor C_m are also depicted in the SCC-based module equalizer. This system also can be regarded as that switches are shared by both the module and cell equalizers. Instead of the half-bridge inverter with a transformer [see Fig. 5(b)], the IVD is introduced to produce a square wave voltage with a peak-to-peak voltage of $V_{mod}L_2/(L_1 + L_2)$, as shown in the inset of Fig. 6.

Since the switching nodes of the IVD-VM-based cell equalizers are tied to capacitors of module equalizers, operations of module and cell equalizers are interdependent; when the IVD-VM-based cell equalizers operate, the module equalizers are also driven by square wave voltages generated in the cell equalizers. Voltages of modules (Modules 1–3) are balanced by the SCC-based switchless module equalizers, while cell voltages in each module are gradually equalized by the IVD-VM-based cell equalizers.

D. Features

The module equalizers in the proposed equalization architecture are essentially switchless, and hence, the switch count can be significantly reduced compared to traditional equalization systems. Since each switch requires several

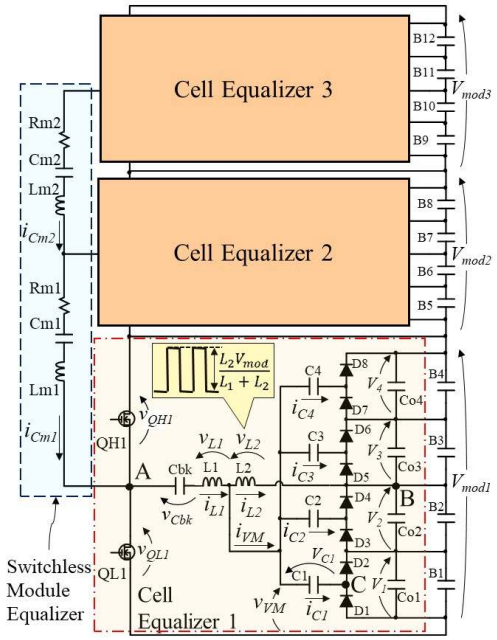


Fig. 6. Proposed modular equalization system using IVD-VM-based cell equalizers and SCC-based switchless module equalizers for three modules, each consisting of four cells connected in series.

ancillary components, including a gate driver IC and its auxiliary power supply, the proposed equalization system contributes to simplifying the circuit.

The transformerless topology of the cell equalizer reduces design difficulty. In general, transformers are not only the bulkiest circuit element in power electronics but also a cumbersome design hurdle because they often have to be custom-designed depending on power rating and input/output voltage ratio. Meanwhile, a variety of inductors can be found in catalogs and are readily available in markets. Although two inductors are necessary for voltage division in each cell equalizer, the transformerless topology lowers the design hurdle and would be beneficial to designers.

The modularity, or extendibility, of the proposed equalization architecture is also good thanks to the adjacent module-to-module SCC-based equalizer. The number of modules connected in series can be arbitrarily extended by adding SCC equalizers and modules each containing a cell equalizer.

To drive the module equalizers in the proposed system, the cell equalizers have to operate to produce square wave voltages even when cell equalization is no longer necessary as all cell voltages are well-equalized. In other words, cell equalizers unnecessarily supply equalization currents to cells. This unnecessary equalization increases processed power as well as associated losses in cell equalizers. In general, an equalization current one-hundredth of a charge/discharge current for a module is considered sufficient to eliminate and preclude voltage imbalance in practical use [34], [35]. This suggests that the loss in cell equalizers is negligibly small compared to that in a charge-discharge regulator and that minor losses due to the unnecessary equalization currents can be justified.

Although modular equalization architectures using the ordinary SCC-based module equalizer is only shown in this paper, other types of adjacent module-to-module equalizers, including resonant and phase-shift SCCs [36], [37], can also be used as long as square wave voltages produced at switching nodes of cell equalizers are available to drive the module equalizers.

E. Comparison with Conventional Modularized Equalizers

The proposed modularized equalization architecture is compared with existing topologies from the viewpoint of component counts in Table I where m is the module count, and n represents the cell count in each module (e.g., the system shown in Fig. 6 corresponds to $m = 3$ and $n = 4$). The switch counts in conventional modularized equalizers are proportional to both m and n because cell and module equalizers are straightforwardly combined without sharing circuit elements. With the multi-winding flyback converter-based cell equalizers [30], the switch count can be independent on n. However, this topology requires m multi-winding transformer each having n secondary windings, likely increasing the design difficulty because precise parameter matching for multiple windings is mandatory to achieve satisfactory equalization performance [38]. The proposed equalization system, on the other hand, can reduce the switch count to only $2m$ without multi-winding transformers, achieving the reduced circuit complexity and design difficulty. A need for numerous passive devices (i.e., inductors, capacitors, and diodes) might be a drawback, but its negative impact is considered very minor as these devices do not require auxiliary circuits nor meticulous design effort unlike

Table I. Comparison between proposed and conventional modularized equalizers in terms of component count

Topology	Module Equalizer	Cell Equalizer	Switch	L	C††	D	Transformer
[26]	Forward Converter	Flyback Converter	mn SSR† + m	-	-	n	$mn + m$
[28]	Multidirectional Multiport Converter	PWM Converter	$2m(n-1) + 2m$	$m(n-1)$	$2m$	-	1 (m Secondary Windings)
[29]	PWM Converter	PWM Converter	$2m(n-1) + 2(m-1)$	$m(n-1) + (m-1)$	-	-	-
[30]	SCC	SCC	$2mn + 2m$	-	$m(n-1) + (m-1)$	-	-
[30]	SCC	Multi-Winding Flyback Converter	$3m$	-	$m-1$	mn	m (n Secondary Windings)
[31]	SCC	Multi-Winding Flyback Converter	$mn + 2m$	-	$m-1$	m	m (n Secondary Windings)
Proposed	SCC	IVD-VM	$2m$	$2m$	$m(n+1) + (m-1)$	$2mn$	-

† Solid-State Relay †† Smoothing capacitors excluded

switches and multi-winding transformers.

III. Operation Analysis

A. Fundamental Operation

The operation of the proposed modular equalization system is basically the combination of the SCC and IVD-VM. Theoretical key operation waveforms and current flow directions when the voltage of B_1, V_1, is the lowest in Module 1 are shown in Figs. 7 and 8, respectively—switches in Module 2 are also illustrated in Fig. 8 to discuss the operation principle. These figures are illustrated with the premise that the voltage of Module 1 is lower than that of Module 2 (i.e., $V_{mod1} < V_{mod2}$) and there is no voltage mismatch in Module 2. Current paths in the cell equalizer for Module 2 are not illustrated for the sake of simplicity. Modes 1–2 and 3–4 correspond to the ON- and OFF-periods of high-side switches (Q_H), respectively. These switches are driven with a 50% fixed duty cycle. At the same time, an ac current of i_{VM} flows toward the VM and is rectified.

It is noteworthy that the SCC should be treated as the one containing inductance L_m, not as an ordinary SCC considering only capacitance and resistance components, because modules are connected using cables in the proposed system (see Section V). In other words, the existence of L_m originating from cables is not negligible. Therefore, the current waveform of C_m, i_{Cm}, reflects the inductive behavior.

Average inductor currents of L_1 and L_2 are zero due to the blocking capacitor C_{bk}. The voltage of C_{bk}, v_{Cbk}, is nearly constant and shows negligibly small ripple if its capacitance is designed to be large enough to avoid resonance with L_1 and L_2. The average voltage at the switching node A is $V_{mod1}/2$ because of the 50% duty cycle operation. From the voltages at the nodes A and B, the average voltage of C_{bk}, V_{Cbk}, can be assumed to be

$$V_{Cbk} = \frac{V_{mod1}}{2} - (V_1 + V_2) \approx 0. \quad (1)$$

Similarly, the average voltage at the node C in the VM is determined to be $V_1/2$ because diodes in the VM also conduct with 50% duty cycle, as can be seen in Figs. 7 and 8. Hence, the average voltage of C_1, V_{C1}, is yielded as

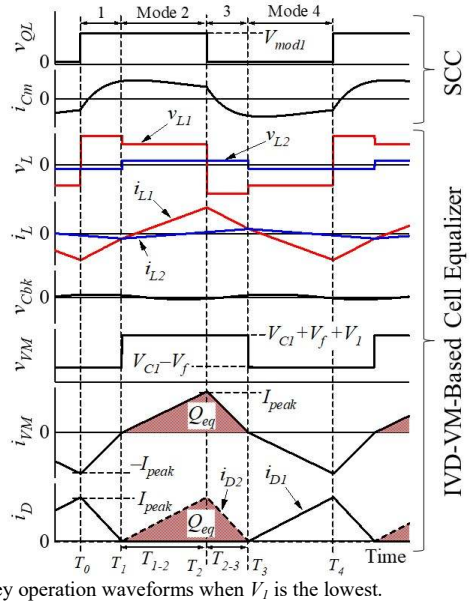


Fig. 7. Key operation waveforms when V_1 is the lowest.

$$V_{C1} = (V_1 + V_2) - \frac{V_1}{2} \approx \frac{V_{mod1} - V_1}{2}. \quad (2)$$

In the following, the voltage at the node B is similarly assumed to be $V_{mod1}/2$.

Mode 1 ($T_0 < t < T_1$) [Fig. 8(a)]: This mode starts as high-side

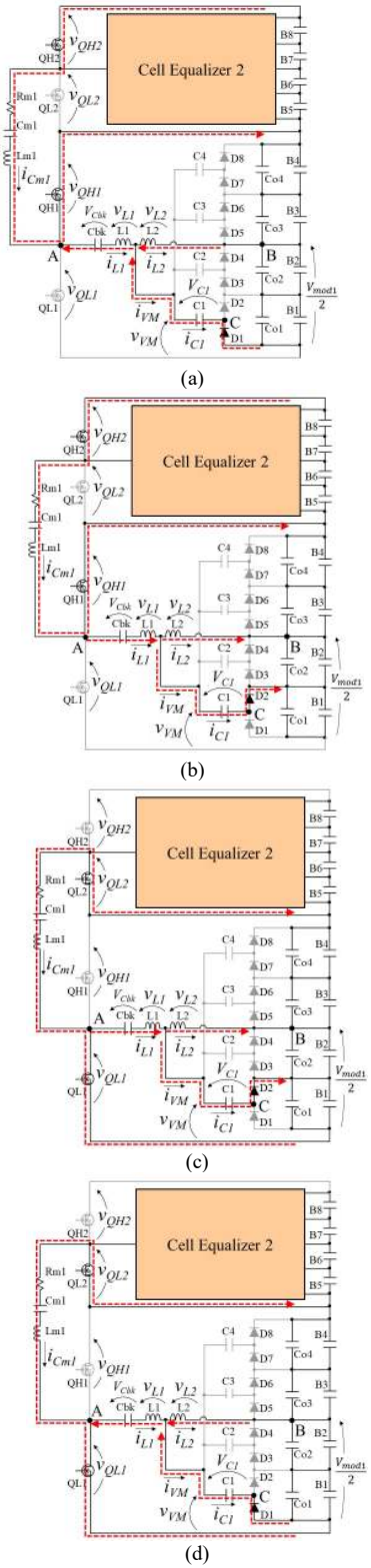


Fig. 8. Current flow directions in (a) Mode 1, (b) Mode 2, (c) Mode 3, and (c) Mode 4.

switches, Q_{H1} and Q_{H2}, are turned on. C_{m1} in the SCC is charged by Module 2, and the current waveform of C_{m1}, i_{Cm1}, is characterized by an LCR response [39] (see Section III-D for detail). The input current of the VM, i_{VM}, corresponds to the difference between i_{L1} and i_{L2}, and therefore,

$$\frac{di_{VM}}{dt} = \frac{di_{L1}}{dt} - \frac{di_{L2}}{dt} = \frac{v_{L1}}{L_1} - \frac{v_{L2}}{L_2}. \quad (3)$$

As i_{VM} is negative and the low-side diode D_1 is conducting, the input voltage of the VM, v_{VM}, is

$$v_{VM} = V_{C1} - V_f = \frac{V_{mod} - V_1}{2} - V_f, \quad (4)$$

where V_f is the forward voltage drop of diodes. As the voltage at the node A is V_{mod1}, the voltages of L_1 and L_2 in Mode 1, v_{L1} and v_{L2}, are given by

$$\begin{cases} v_{L1} = V_{mod1} - v_{Cbk} - v_{VM} = \dfrac{V_{mod} + V_1}{2} + V_f \\ v_{L2} = v_{VM} - \dfrac{V_{mod1}}{2} = \dfrac{-V_1}{2} - V_f \end{cases}. \quad (5)$$

The slope of i_{VM} in this mode is yielded by substituting (5) into (3), as

$$\frac{di_{VM.1}}{dt} = \frac{V_{mod1}L_2 + V_1(L_1 + L_2) - 2V_f(L_1 + L_2)}{2L_1L_2}. \quad (6)$$

Mode 2 ($T_1 < t < T_2$) [Fig. 8(b)]: This mode starts when i_{L1} overtakes i_{L2}, and i_{VM} becomes positive. The behavior of i_{Cm1} in this mode is identical to that in Mode 1. In the VM, on the other hand, the high-side diode D_2 begins to conduct, and hence,

$$v_{VM} = V_{C1} + V_f + V_1 = \frac{V_{mod} + V_1}{2} + V_f, \quad (7)$$

$$\begin{cases} v_{L1} = V_{mod1} - v_{Cbk} - v_{VM} = \dfrac{V_{mod} - V_1}{2} - V_f \\ v_{L2} = v_{VM} - \dfrac{V_{mod1}}{2} = \dfrac{V_1}{2} + V_f \end{cases}. \quad (8)$$

From (3) and (8), the slope of i_{VM} in Mode 2 is obtained as

$$\frac{di_{VM.2}}{dt} = \frac{V_{mod1}L_2 - V_1(L_1 + L_2) - 2V_f(L_1 + L_2)}{2L_1L_2}. \quad (9)$$

Mode 3 ($T_2 < t < T_3$) [Fig. 8(c)]: This operation mode is symmetric to Mode 1. The low-side switches, Q_{L1} and Q_{L2}, are turned ON, and v_{QL} becomes zero. At the same time, C_{m1} starts discharging to Module 1. In the VM, the high-side diode D_2 is still conducting, and therefore, v_{VM} in Mode 3 is identical to that in Mode 2 [see (7)]. Meanwhile, v_{L1} swings as v_{QL} becomes zero;

$$\begin{cases} v_{L1} = -v_{Cbk} - v_{VM} = \dfrac{-V_{mod} - V_1}{2} - V_f \\ v_{L2} = v_{VM} - \dfrac{V_{mod1}}{2} = \dfrac{V_1}{2} + V_f \end{cases}. \quad (10)$$

Since this mode is symmetric to Mode 1, the slope of i_{VM} is identical to (5), but its sign is negative;

$$\frac{di_{VM.3}}{dt} = -\frac{di_{VM.1}}{dt}. \quad (11)$$

Mode 4 ($T_3 < t < T_4$) [Fig. 8(d)]: This mode is symmetric to Mode 2. As the polarity of i_{VM} changes to negative, the low-side diode D_1 conducts and v_{VM} is identical to that in Mode 1 [see (4)]. The swing of v_{VM} also changes v_{L1} and v_{L2}, as

$$\begin{cases} v_{L1} = -v_{Cbk} - v_{VM} = \dfrac{-V_{mod} + V_1}{2} + V_f \\ v_{L2} = v_{VM} - \dfrac{V_{mod1}}{2} = -\dfrac{V_1}{2} - V_f \end{cases}. \quad (12)$$

The slope of i_{VM} is identical to (9), but its polarity is negative;

$$\frac{di_{VM.4}}{dt} = -\frac{di_{VM.2}}{dt}. \quad (13)$$

In summary, the waveforms of the SCC in the proposed modular equalization system are identical to those of traditional one [39], suggesting that the operations of the SCC and VM are independent. Voltages of inductors, v_{L1} and v_{L2}, are dependent on not only switching states but also the relationship between i_{L1} and i_{L2}. As the ac current of i_{VM} flows, the high- and low-side diodes connected in parallel with the least charged cell alternately conduct, whereas others do not. Hence, an equalization current flows toward the least charged cell only.

B. Modeling of IVD-VM Cell Equalizer

An equalization current supplied to B_1 from the VM is equal to an average current of either diode (D_1 or D_2). Since the sum of the diode currents, i_{D1} and i_{D2}, are identical to the absolute value of i_{VM} (see Fig. 7), i_{VM} averaged over half the switching period or the charge delivered to B_1, Q_{eq} (designated in Fig. 7), can derive the equalization current supplied to cells.

To obtain Q_{eq}, mode lengths and the peak value of i_{VM}, I_{peak}, need to be determined. The sum of lengths of Modes 2 and 3, $T_{1\text{-}2}$ and $T_{2\text{-}3}$, is equal to $T_s/2$ because of the operation symmetry. From (6), (9), and (11), $T_{1\text{-}2}$ and $T_{2\text{-}3}$ are expressed as

$$\begin{aligned} T_{1-2}:T_{2-3} &= \frac{di_{VM.3}}{dt}:\frac{di_{VM.2}}{dt} \\ &= V_{mod1}L_2 + V_1(L_1 + L_2) - 2V_f(L_1 + L_2):V_{mod1}L_2 \\ &\quad - V_1(L_1 + L_2) - 2V_f(L_1 + L_2). \end{aligned} \quad (14)$$

The peak current of i_{VM}, I_{peak}, is yielded as shown at the bottom of this page.

The equalization current I_{eq} is

$$I_{eq} = \frac{Q_{eq}}{T_s} = \frac{\frac{1}{2}\frac{T_s}{2}I_{peak}}{T_s} = \frac{I_{peak}}{4}. \quad (16)$$

It is noted that the module and cell voltages are generalized as V_{mod} and V_i (i = 1…4) in this equation. Although I_{eq} is dependent on V_{mod}, V_i, and V_f, the influence of V_i and V_f on I_{eq} is very minor because V_{mod} is rather larger than V_i and V_f (e.g., $V_{mod}/6 \approx V_i > V_f$ for modules consisting of six cells connected in

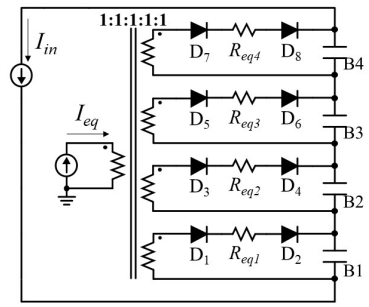


Fig. 9. DC equivalent circuit of IVD-VM cell equalizer.

$$I_{peak} = \frac{di_{VM.2}}{dt}T_{1-2} = \frac{(V_{mod1}L_2)^2 - 4V_{mod}V_fL_2(L_1 + L_2) - \{V_1(L_1 + L_2)\}^2 + \{2V_f(L_1 + L_2)\}^2}{8V_{mod}L_1L_2^2 - 16V_f(L_1 + L_2)L_1L_2}T_s. \quad (15)$$

series). Therefore, I_{eq} is nearly constant at any value of V_i, as will be demonstrated in the experimental section.

The equalization current I_{eq} dictates the equalization capability—the larger the value of I_{eq}, the faster will be the equalization. In general, an equalization current one-hundredth of a charge-discharge current is considered sufficient to preclude or eliminate voltage imbalance [34], [35]. Hence, the value of I_{eq} should be properly determined depending on applications and cycling conditions.

The average input current of the equalizer I_{in} can be derived by integrating i_{L1} over Modes 1 and 2. A mathematical expression of i_{L1}, however, is very complicated, and hence, I_{in} is approximated based on energy conservation law to simplify the analysis. Assuming the equalizer is ideal with no losses, I_{in} can be approximated as

$$I_{in} \approx \frac{I_{eq}V_i}{V_{mod}}. \tag{17}$$

A dc equivalent circuit of the half-bridge inverter with the VM has been derived in the previous work [15]. The proposed IVD-VM equalizer can also be expressed using the identical form of the equivalent circuit, as shown in Fig. 9. All the cells are connected to the current source I_{eq} [see (16)] through the ideal multi-winding transformer, diodes, and equivalent resistor R_{eqi} (i = 1…4), whose value has been mathematically modeled in the previous work [15], as

$$R_{eqi} = 2(r_i + r_D) + \frac{1}{C_i f}, \tag{18}$$

where r_i is the ESR of C_i and r_D is the diode resistance.

All the cells equally provide I_{in} [see (17)] for the input of the equalizer, while I_{eq} preferentially flows toward a cell having the lowest voltage under voltage-imbalanced conditions. Thus, the IVD-VM cell equalizer redistributes energies of cells in the form of I_{in} and I_{eq}, and cell voltages are automatically balanced as time elapsed.

C. Operation Criterion of IVD-VM Cell Equalizer

In order for the VM to supply equalization current, i_{VM} must flow in Modes 2 and 4 [see Figs. 8(b) and (d)] so that diodes conduct. In the operations discussed in the previous subsection, v_{L2} is clumped by v_{VM} and V_{mod}, as expressed by (5), (8), (10), and (12). In the case that i_{VM} does not flow, the voltage applied between nodes A and B is simply divided by L_1 and L_2, and v_{L2} is

$$v_{L2} = \begin{cases} \frac{V_{mod}}{2}\frac{L_2}{L_1+L_2} & \text{(Modes 1 and 2)} \\ -\frac{V_{mod}}{2}\frac{L_2}{L_1+L_2} & \text{(Modes 3 and 4)} \end{cases}. \tag{19}$$

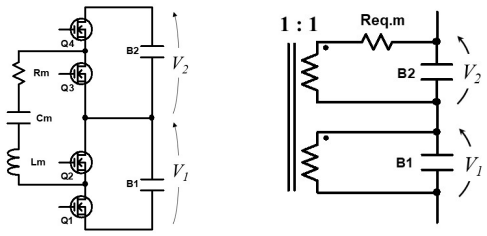
In order for i_{VM} to flow in Modes 2 and 4, the following relationship among v_{VM}, v_{L2}, and V_{mod1} needs to be satisfied;

$$v_{VM} \begin{cases} > v_{L2} + \frac{V_{mod}}{2} & \text{(Mode 2)} \\ < v_{L2} + \frac{V_{mod}}{2} & \text{(Mode 4)} \end{cases}. \tag{20}$$

Substitution of (5) and (8) into (20) produces the operation criterion

$$\frac{L_2}{L_1+L_2} > \frac{V_i + 2V_f}{V_{mod}}. \tag{21}$$

Thus, L_1 and L_2 need to be determined considering the ratio of the module voltage (V_{mod}) and cell voltage (V_i).



(a) (b)

Fig. 10. (a) Basic SCC including ESR and ESL, (b) dc equivalent circuit of SCC.

D. Switched Capacitor Converter (SCC)-Based Module Equalizer

In general, an SCC is well known to be expressed using an equivalent resistance, as shown in Fig. 10. A charge-discharge operation of a capacitor is equivalently expressed using an equivalent resistor and an ideal transformer with unity turns ratio. The operation of an SCC including an ESL [see Fig. 10(a)] has been thoroughly analyzed in the previous work [39]. According to this reference, the equivalent resistance, $R_{eq.m}$, is given by

$$R_{eq.m} = \frac{1}{C_m f_s}\left[1 + \frac{s_1 e^{s_2 d_1/f_s} - s_2 e^{s_1 d_1/f_s}}{s_1 - s_2 - (s_1 e^{s_2 d_1/f_s} - s_2 e^{s_1 d_1/f_s})} + \frac{s_1 e^{s_2 d_2/f_s} - s_2 e^{s_1 d_2/f_s}}{s_1 - s_2 - (s_1 e^{s_2 d_2/f_s} - s_2 e^{s_1 d_2/f_s})}\right], \tag{22}$$

where

$$\begin{cases} s_1 = -\frac{R_m}{2L_m} + \sqrt{\frac{R_m{}^2}{4L_m{}^2} - \frac{1}{L_m C_m}} \\ s_2 = -\frac{R_m}{2L_m} - \sqrt{\frac{R_m{}^2}{4L_m{}^2} - \frac{1}{L_m C_m}} \end{cases}, \tag{23}$$

where L_m is the cable inductance, and R_m is the total resistance of the current loop including the ESR of C_m.

As the dc equivalent circuit suggests, the time constant τ formed by $R_{eq.m}$ and the total capacitance of B_1 and B_2 dictates the equalization speed of the SCC-based module equalizer;

$$\tau = \frac{C_{B1}C_{B2}}{C_{B1}+C_{B2}} R_{eq.m}, \tag{24}$$

where C_{B1} and C_{B2} are the capacitance of B_1 and B_2, respectively. Similar to typical CR response characteristics, the smaller the value of τ, the faster will be the equalization.

IV. DC Equivalent Circuit and its Simulation Results

A. Derivation of DC Equivalent Circuit

By combining the equivalent circuits of the IVD-VM and SCC shown in Figs. 9 and 10(b), respectively, the dc equivalent circuit of the proposed modular equalization system as a whole can be derived as shown in Fig. 11. Voltages of adjacent modules are equalized by charging and discharging each other through the ideal transformer and $R_{eq.m}$. Therefore, the speed of module equalization is dependent on the value of $R_{eq\text{-}m}$, as (24) indicates. Meanwhile, cell voltages in each module are gradually equalized by energy redistribution in the form of $I_{eq.i}$ and $I_{in.i}$ a(i = 1 or 2) as discussed in Section III-C. Therefore,

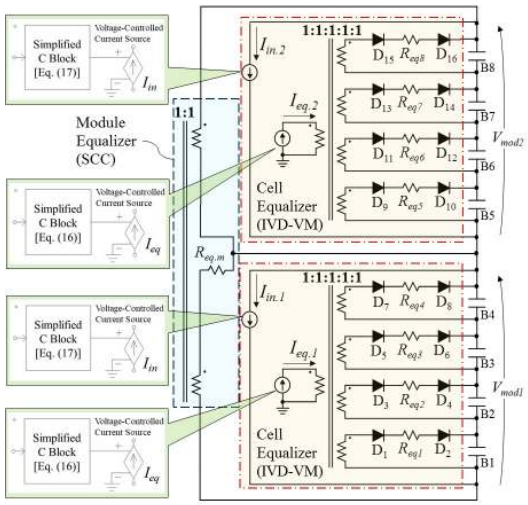


Fig. 11. DC equivalent circuit of the modular equalization architecture for two modules.

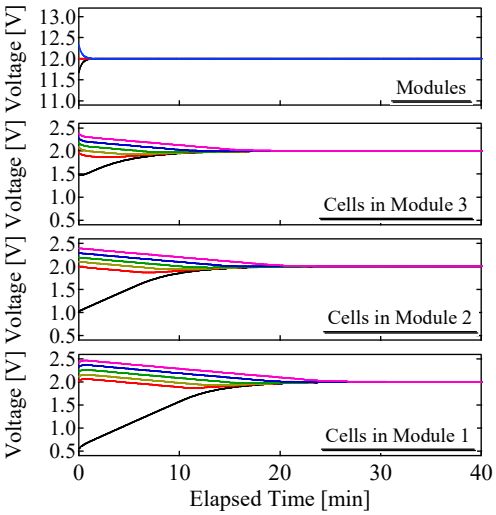


Fig. 12. Equalization profiles of derived dc equivalent circuit.

the speed of cell equalization is determined by the values of $I_{eq.i}$ and $I_{in.i}$.

B. Simulation-Based Equalization

To validate the derived dc equivalent circuit, the simulation-based equalization was performed for three modules, each consisting of six cells. The analysis was carried out using PSIM with a time step of 1.0 s, and I_{eq} and I_{in} were modeled as the combination of a voltage-controlled current source and simplified C-block, as depicted in the inset of Fig. 11. According to the component values used for the prototype, which will be shown in Table II in the next section, the values of R_{eqi} and $R_{eq.m}$ were determined to be 353 mΩ and 905 mΩ based on (18) and (22), respectively. I_{eq} and I_{in} were programmed to obey (16) and (17). Capacitors with a capacitance of 400 F were used as cells, and their initial voltages were intentionally imbalanced.

The resultant equalization profiles are shown in Fig. 12. Module voltages were immediately equalized to be 12.0 V thanks to the relatively powerful SCC-based module equalizer. Meanwhile, cell voltages in each module were gradually balanced by the IVD-VM-based cell equalizers. All the cell voltages converged to the same voltage of 2.0 V.

V. Experimental Results

A. Prototype

The prototype of a module consisting of six EDLC cells with an IVD-VM cell equalizer was built, as shown in Fig. 13. Table II lists the circuit elements used for the prototype. EDLCs with a capacitance of 400 F at a rated charge voltage of 2.5 V were mounted on the printed circuit board (PCB). The values of L_1 and L_2 were determined so that I_{eq} under the voltage imbalanced condition be approximately 1.0 A, according to (16) at V_{mod} = 15 V and f_s = 100 kHz. The capacitor for the SCC-based module equalizer was also mounted on the PCB, and modules were connected using cables. R_m and L_m were measured to be approximately 217 mΩ and 12.7 nH, respectively. Ceramic capacitors with 47 μF were selected so that the time constant τ of the SCC-based module equalizer [see (24)] be approximately 60 s, with considering cable impedance. Gating signals with 50% duty cycle were applied to gate drivers by a function generator (AFG1000, Tektronix).

B. Characteristics of IVD-VM-Based Cell Equalizer

The fundamental characteristics of the prototype as an IVD-VM equalizer was measured using the experimental setup shown in Fig. 14(a). The input and output of the equalizer (i.e., the switch leg and output smoothing capacitors) were separated, and an external power supply V_{ext} = 15 V was connected to the input. EDLCs were removed, and smoothing capacitors alone sustained V_1–V_6. A variable resistor was connected to the selectable tap, with which operation modes under voltage-balanced and -imbalanced conditions can be emulated. Operation modes under the voltage-imbalanced condition shown in Fig. 8 can be emulated with the tap X. With the tap Y

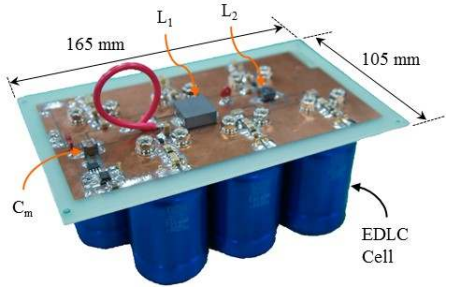


Fig. 13. Photograph of cell equalizer prototype for six EDLCs.

Table II. Component values used for the prototype

Component	Value, Part Number
C_{m1}, C_{m2}	Ceramic Capacitor, 33μF
Q_{L1}–Q_{L3}, Q_{H1}–Q_{H3}	Dual MOSFET, IRF7341, R_{on} = 50 mΩ
L_1	4.7 μH, 16 mΩ
L_2	8.2 μH, 60 mΩ
C_{bk}	Ceramic Capacitor, 100 μF
C_1–C_6	Ceramic Capacitor, 94 μF
D_1–D_{12}	Dual Schottky Barrier Diode, SBS811, V_f = 0.3
C_{o1}–C_{o6}	Ceramic Capacitor, 740 μF
Gate Driver	IRF2184S

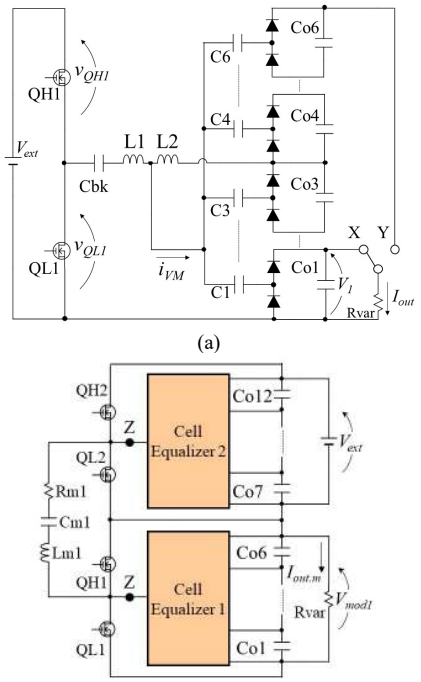


Fig. 14. Experimental setup for characteristics measurement for (a) IVC-VM-based cell equalizer and (b) SCC-based module equalizer.

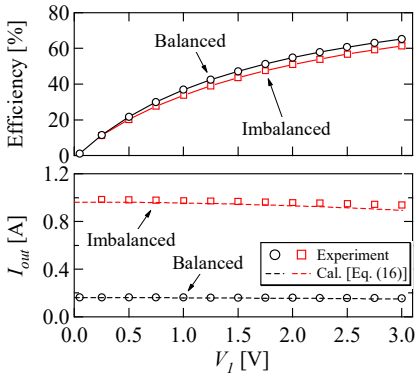


Fig. 15. Measured characteristics of IVD-VM-based cell equalizer.

selected, on the other hand, the equalizer operates as if there is no voltage imbalance. The value of V_{ext} corresponds to the module voltage V_{mod} in the practical case.

The measured output characteristics of the IVD-VM cell equalizer are shown in Fig. 15. The output current I_{out} of R_{var} was nearly constant and independent on the cell voltage V_1. This is because I_{eq} [see (15) and (16)] is chiefly dependent on V_{mod} (= V_{ext}) and is nearly independent on the cell voltage, as discussed in Section III-B. I_{out} under the voltage imbalanced condition was six times greater than that under the voltage balanced condition because I_{eq} was independent on whether cell voltages are balanced and was equally distributed to six smoothing capacitors C_{o1}–C_{o6} under voltage-balanced condition. The experimental and theoretical characteristics of I_{out} of (16) were in good agreement, verifying the derived mathematical model.

In the range of V_1 lower than 3.0 V, which is a typical voltage range of EDLCs, measured efficiencies monotonically increased with V_1. This tendency suggested that the diode

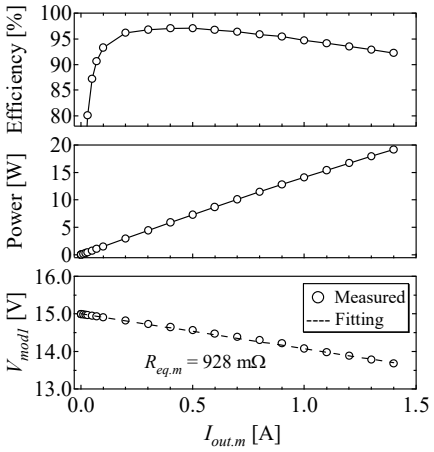


Fig. 16. Measured characteristic of SCC-based module equalizer.

conduction loss was the most dominant loss factor in the voltage range lower than 3.0 V and that the loss portion taken by the diode forward voltage drop became less significant as V_1 increased. The efficiency under the voltage-balanced condition was slightly higher than that under voltage-imbalance condition. I_{eq} was equally distributed to C_{o1}–C_{o6} under the voltage-balanced condition, hence reducing RMS currents as well as Joule losses associated with capacitors and diodes in the VM. The efficiency at V_1 = 3.0 V under the balanced condition was as high as 65.3% and was comparable to conventional VM-based equalizers [15].

C. Characteristics of SCC-Based Module Equalizer

Characteristics as an SCC-based module equalizer were measured with the setup shown in Fig. 14(b). Nodes Z are broken to disable the IVD-VM cell equalizers, and all cells were removed. An external power supply V_{ext} = 15 V was connected to the C_{o7}–C_{o12}, while C_{o1}–C_{o6} were tied to a variable resistor R_{var}. $I_{out.m}$ corresponds to an equalization current for Module 1.

Measured characteristics are shown in Fig. 16. As $I_{out.m}$ increased, V_{mod1} linearly decreased, verifying that the output characteristics of the SCC is characterized as an equivalent resistance. From the slope of the measured characteristic, the value of $R_{eq.m}$ was determined to be 928 mΩ. The measured efficiency was higher than 90% in the output power region greater than 1.0 W.

D. Equalization Test for Three EDLC Modules

Three EDLC modules, each containing six cells connected in series, were used for the equalization experiment, as shown in Fig. 17. The prototype PCBs were connected in series using cables. The equalization test was performed from the voltage-imbalanced condition—cell voltages as well as module voltages

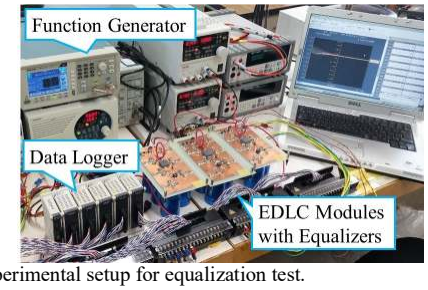


Fig. 17. Experimental setup for equalization test.

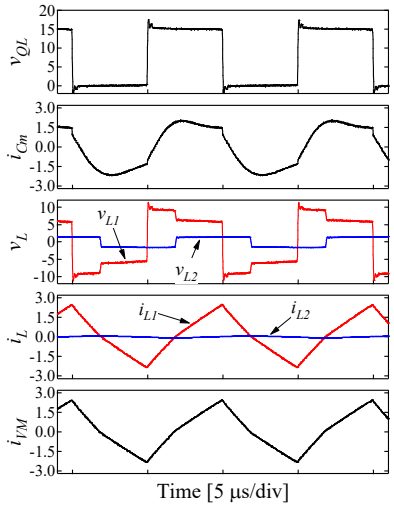


Fig. 18. Measured waveforms when V_1 is the lowest.

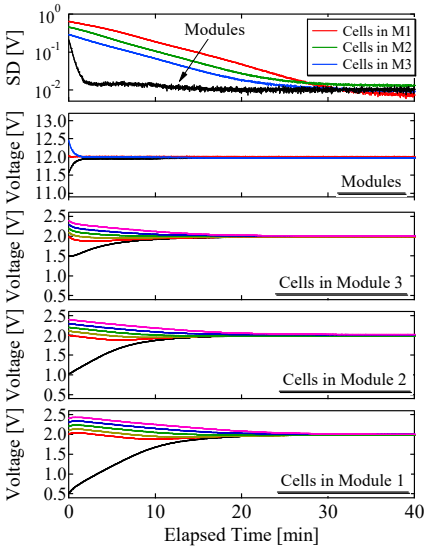


Fig. 19. Experimental equalization profiles.

were severely imbalanced in order to accentuate the equalization performance of the proposed equalization system. Module and cell voltages during equalization were measured using a data logger (NR-500, KEYENCE).

The measured key operation waveforms during the equalization test are shown in Fig. 18. These waveforms matched well with theoretical ones shown in Fig. 7, verifying the operation principle of the proposed modular equalization system.

The resultant equalization profiles are shown in Fig. 19. Cell voltages in each module were gradually equalized by the IVD-VM-based cell equalizer. Meanwhile, module voltages were immediately balanced by the SCC-based module equalizer since the module equalizer was designed more powerful than the cell equalizers. Standard deviations (SDs) of module and cell voltages decreased down to as low as approximately 10 mV at the end of the experiment, demonstrating the equalization performance. The experimental equalization profiles matched well with the simulation results of the dc equivalent circuit (see Fig. 12), verifying the theoretical analysis as well as the derived dc equivalent circuit.

VI. Conclusions

The modular equalization architecture for series-connected EDLC modules, each also consisting of multiple cells connected in series, has been proposed in this paper. The square wave voltage generated at the switching node of the IVD-VM-based cell equalizer is utilized to drive the SCC-based module equalizer. The IVD-VM-based cell equalizers and SCC-based module equalizers can be integrated with sharing switches, thus halving the total switch count in comparison with traditional modular systems employing cell and module equalizers separately. In addition, the proposed modular system offers good modularity as the number of modules can be arbitrarily extended with adding modules with SCC-based module equalizers.

The detailed operation analysis was performed mainly for the IVD-VM-based cell equalizer, followed by the derivation of the dc equivalent circuit. The equalization speed of the IVD-VM-based equalizer is characterized by the equalization current I_{eq}, while that of the SCC-based module equalizer is dictated by the time constant τ formed by the equivalent resistance and total capacitance of EDLCs.

The experimental equalization test for three EDLC modules, each consisting of six cells connected in series, was performed from the initially voltage-imbalanced condition using the prototype of the proposed system. The module and cell voltages were balanced at a different rate, verifying the proposed modular equalization architecture concept. The experimental equalization profiles matched well with those of the simulation analysis based on the dc equivalent circuit, verifying the derived dc equivalent circuit as well as the operation analysis.

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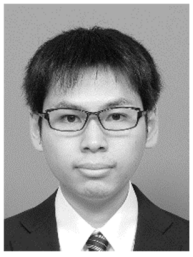

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