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Transformer-Less Bidirectional PWM Converter Integrating Voltage Multiplier-Based Cell Voltage Equalizer for Series-Connected Electric Double-Layer Capacitors

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***Abstract*— In the traditional energy storage systems consisting of series-connected energy storage cells such as electric double-layer capacitors (EDLCs), not only a bidirectional PWM converter but also a cell voltage equalizer is required. The system is prone to complexity as two converters (i.e., the bidirectional converter and cell voltage equalizer) are separately necessary. This paper proposes the transformer-less bidirectional PWM converter integrating the voltage multiplier-based cell voltage equalizer. An inductor in a conventional bidirectional PWM converter is replaced with series-connected inductors in the proposed converter in order to generate square wave voltage with an arbitrary amplitude, by which the voltage multiplier is driven. The charge-discharge cycling test for nine EDLCs connected in series was performed using the proposed integrated converter from a voltage-imbalanced condition. The voltage imbalance was gradually eliminated during charge-discharge cycling, demonstrating the integrated functions.**

***Index Terms*— Electric double-layer capacitor (EDLC), integrated converter, PWM converter, voltage equalization, voltage multiplier**

I. INTRODUCTION

In recent years, electric double-layer capacitors (EDLCs), an energy storage device with a high-power capability and long life performance, play important roles in various applications such as regenerative energy systems, hybrid electric vehicles, and uninterruptible power supplies. However, since a voltage of one single energy storage cell (hereafter simply call 'cell') is low, multiple cells need to be connected in series to form a string to meet voltage requirements of loads. Voltages of series-connected cells in such systems, however, tend to be gradually imbalanced due to non-uniform individual cell characteristics in terms of capacitance, internal impedance, and self-discharge rate. In such voltage-imbalanced systems, not only are cells with high/low voltages over-charged/-discharged during charging/discharging, respectively, but also the chargeable and dischargeable energy of the system as a whole is greatly reduced [1], [2].

Various kinds of cell voltage equalizers have been proposed to address the voltage imbalance issues [3]. With adjacent cell-to-cell equalizers, such as bidirectional PWM converters [4]–[11] and switched capacitor converters [12]–[21], numerous equalizers in proportion to the number of cells connected in series are necessary, resulting in increased system complexity and cost. Meanwhile, the number of equalizers can be reduced with equalizers using selection switches [22]–[29] and string-to-cell equalizers based on multi-winding converters [30]–[33], multi-stacked buck-boost converters [34], voltage multipliers [35], [36]. Since the adjacent cell-to-cell equalizers and equalizers with selection switches require numerous switches in proportion to the number of cells connected in series, the string-to-cell equalizers are a preferable choice from the viewpoint of system simplification.

A schematic diagram of a conventional energy storage system with a string-to-cell equalizer is illustrated in Fig. 1(a). Although the equalizer itself is simple, there are two separate components (i.e., the bidirectional PWM converter and equalizer) are necessary. If these two components were to be integrated into a single unit, the system would be even simpler. The bidirectional PWM converter integrating cell voltage equalizer has been proposed to realize the integration as well as system simplification [37]–[39], as shown in Fig. 1(b). The integrated converter offers two functions of the bidirectional power conversion and cell voltage equalization, and therefore,

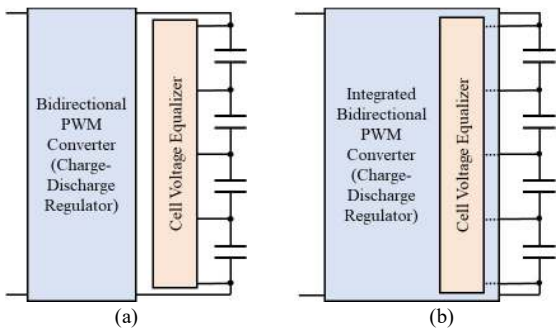

Fig. 1. Energy storage systems with voltage equalizer: (a) Conventional system with string-to-cell equalizer, (b) proposed integrated converter systems.

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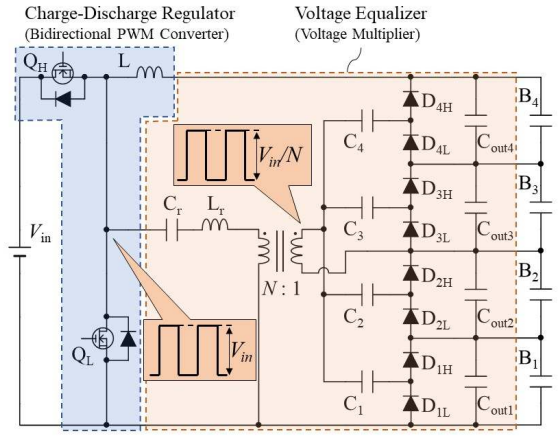
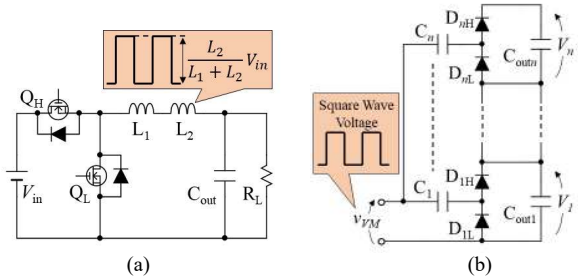


Fig. 2. Conventional integrated converter based on bidirectional PWM converter and voltage multiplier [38].

the equalizer is equivalently included in the bidirectional converter.

The integrated converter proposed in [38] is shown in Fig. 2. The equalizer in the integrated converter is basically a voltage multiplier with a simple circuit configuration, and a transformer has been used in order to produce a square wave voltage with an arbitrary amplitude (see insets in Fig. 2), by which the voltage multiplier is driven. Since the square wave voltage generated at the switching node of the PWM converter is utilized to drive the voltage multiplier, the equalizer itself is essentially switchless. Although the conventional integrated converter is very simple, the existence of the transformer poses design challenges from the viewpoint of design flexibility and extendibility. Transformers are usually a customized component, and its turns ratio and core must be properly determined according to specifications and requirements, such as the number of cells connected in series and input voltage of the converter. For example, if the number of cells is doubled from four to eight, the transformer needs to be redesigned by doubling the turns ratio and probably reselecting a proper core. It is a daunting task because practical transformer design is far more difficult than simply selecting discrete components from a product catalog.

This paper presents the extended and fully developed work about the transformer-less bidirectional PWM converter integrating a voltage multiplier-based cell voltage equalizer that was proposed in the previous work [40]; thorough analysis, derivation of a dc equivalent circuit, and more detailed experimental and simulation results will be presented in this paper. Thanks to the transformer-less topology, the design flexibility and circuit extendibility can be considerably



(a) (b)

Fig. 3. Key elements for proposed integrated converter: (a) Bidirectional PWM converter with inductor-based voltage divider, (b) voltage multiplier.

improved compared with the conventional integrated converter. The rest of this paper is organized as follows. Section II presents the derivation procedure and discusses the major benefits of the proposed integrated converter. Section III performs the detailed operation analysis, followed by the explanation of the voltage equalization mechanism and establishment of operational criterion. In Section IV, the dc equivalent circuit of the proposed converter is derived. In Section V, the experimental result of the charge-discharge cycling test for nine EDLCs connected in series using the prototype are presented and are compared with simulation results of the dc equivalent circuit.

II. Transformer-Less Integrated Converter

A. Circuit Derivation

The proposed integrated converter is derived from the combination of two converters shown in Fig. 3. The circuit configuration of the bidirectional PWM converter, shown in Fig. 3(a), is basically the same as the conventional PWM buck converter—an inductor in the conventional PWM converter is replaced with two inductors (L_1 and L_2) connected in series. Similar to a conventional PWM converter, a square wave having a peak-to-peak voltage equal to the input voltage V_{in} is generated across two inductors of L_1 and L_2. Therefore, the square wave voltage generated across the series-connected inductors is divided by L_1 and L_2, as depicted in the inset of Fig. 3(a).

The voltage multiplier shown in Fig. 3(b) is driven by square wave voltage. As an ac current/voltage wave is applied to the input of the voltage multiplier, voltages of smoothing capacitors C_{out1}–C_{outn}, V_1–V_n, are automatically unified, allowing automatic voltage equalization if cells are connected in parallel with C_{out1}–C_{outn}.

By utilizing the square wave voltage generated across L_2 to drive the voltage multiplier, the proposed integrated converter can be derived, as shown in Fig. 4. A transformer has been used in the conventional integrated converter (see Fig. 2) in order to produce a square wave with an arbitrary peak-to-peak voltage, by which the voltage multiplier is driven [38]. In the proposed integrated converter, on the other hand, the peak-to-peak voltage can be adjusted by the inductance ratio of L_1 and L_2. Thanks to the inductor-based voltage divider, the transformer is

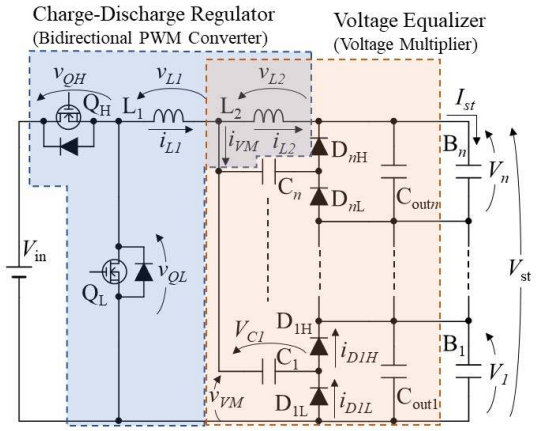


Fig. 4. Proposed transformer-less integrated converter for n cells connected in series.

Table I. Comparison between conventional and proposed equalizer in term of component count.

Topology		Switch	L	C†††	D	Transformer
Adjacent Cell-to-Cell Equalizer	[5], [6]	$2(n-1)$	$n-1$	-	-	-
	[7], [8]	$2(n-1)$	$2(n-1)$	$n-1$	-	-
	[13]	$2n$	-	$2n-3$	-	-
	[14], [17]	$2n$	-	$n-1$	-	-
Equalizer with Selection Switches	[22]	2 and $2n$ †	-	-	2	2
	[23]	$n+5$†	1	1	-	-
	[24]	5 and $4(n+1)$†	2	2	5	-
	[25]	$2(n+1)$	1	-	$2(n+1)$	-
	[26]	2 and $2n$ †	1	1	-	-
	[28]	2 and $2n$ †	-	-	2	2
	[29]	$2(n-1)$	-	-	1	1
String-to-Cell Equalizer	[30]	n†	-	-	-	1††
	[31]	2	-	-	$n+2$	1††
	[32]	2	1	2	$4n$	1††
	[34]	1	$n+1$	n	n	-
	[35]	2	-	$n+2$	$2n$	1
	[36]	2	-	$n+2$	$2n$	1
Integrated Converter	[37]	2	3	1	$2(n+1)$	1 and 1††
	[38]	2	1	$n+1$	$2n$	1
	Proposed	2	2	n	$2n$	-

† Bidirectional switch (relay) ††† Smoothing capacitors excluded
†† Multi-winding transformer

no longer necessary to drive the voltage multiplier, improving the design flexibility and extendibility.

B. Major Features

The proposed integrated converter can be derived with no additional switch because the voltage equalizer in Fig. 3(b) is essentially a switchless circuit. Therefore, not only is the system-level simplification feasible by the integration but also the circuit-level simplification can be achieved by reducing the switch count compared to the conventional system using separate converters [see Fig. 1(a)]. In general, the switch count is a good metric to represent the circuit complexity because each switch requires several ancillary circuit elements, including a gate driver IC and its auxiliary power supply. The switch count in the proposed converter is only two, whereas the conventional system [Fig. 1(a)] requires four in total—both the converter and equalizer need two switches.

The lack of a transformer also contributes to ease circuit design. As mentioned in Section I, if specifications (e.g., the numbers of cells connected in series) are changed, a transformer in the conventional integrated converter needs to be redesigned by adjusting a turns ratio and reselecting a proper core. In contrast, a variety of inductors are readily available in markets and can be found in product catalogs, and hence, customized design is no longer necessary for the proposed transformer-less integrated converter. Although inductors should be properly selected with considering various aspects, such as inductance, current rating, etc., the design difficulty can be significantly reduced because designers are freed from cumbersome transformer design.

As mentioned above, the square wave voltage is generated across L_2 as long as the PWM converter operates. In other words, even when cell voltages are unified and equalization is no longer necessary, the voltage multiplier is always driven, unnecessarily supplying equalization currents for cells. This unnecessary equalization naturally increases the processed power in the converter as well as the associated loss. However, in general, an equalization current necessary in practical use is very small as one-hundredth of the charging/discharging current is considered sufficient to eliminate voltage imbalance [42], [43]. Therefore, the loss associated with the voltage multiplier is negligibly small when compared to a relatively large loss in the PWM converter.

The drawback of the integrated converter is that optimization for individual performance of the PWM converter and voltage multiplier is infeasible due to the integration. Shared two inductors should be optimally designed for the more important converter (i.e., the PWM converter because of its larger processing power), and the performance of the voltage multiplier is necessarily compromised to some extent. Hence, the integrated converter is considered best suitable for small-scale applications where system simplification and cost saving are prioritized over performance optimization.

C. Comparison with Conventional Equalizers

The component counts necessary in the proposed integrated converter are compared with those in conventional equalizers in Table I, in which n is the number of cells connected in series. Various kinds of equalizers are roughly categorized into four groups: adjacent cell-to-cell equalizers, equalizers with selection switches, string-to-cell equalizers, and integrated converters.

The adjacent cell-to-cell equalizers require numerous switches and passive components, hence increasing the circuit complexity, cost, and volume. In addition, the energy transfer of adjacent cell-to-cell equalizer is limited only between two adjacent cells, resulting in relatively slow equalization speed and low efficiency due to collective power conversion losses—energy from the most charged cell in a string may have to traverse multiple equalizers and cells before reaching the least charged cell.

Equalizers with selection switches, on the other hand, can dramatically reduce the passive component counts, and therefore are suitable for large-scale applications where the

Table II. Estimated cost of prototype's equalizer.

	Quantity	Unit Price [$]	Subtotal [$]	Total [$]
Inductor L_2, 100 µH (Murata)	1	0.52	0.52	6.78
Ceramic Capacitor, 22 µF, 25 V (Murata)	9	0.14	1.23	
Ceramic Capacitor, 100 µF, 6.3 V (Murata)	18	0.17	3.11	
Schottky Diode, PMEG1030EH (NXP Semiconductors)	18	0.11	1.91	

reduced passive component counts are attractive from the viewpoint of circuit miniaturization. In addition, direct cell-to-cell power transfer is feasible with selection switches [22]–[29], allowing fast and efficient equalization performance. However, not only are numerous switches or bidirectional switches necessary but also relatively complex equalization algorithms based on individual cell voltage measurement are mandatory to perform equalization.

Necessary switch counts can be reduced to a few with the string-to-cell equalizers, hence dramatically simplifying the circuit compared to other topologies. Energies of cells are redistributed from a string to the least charged cell via an equalizer, and therefore, an equalization speed of string-to-cell equalizers is inevitably slower than that of direct cell-to-cell equalizers using selection switches. Although simplified circuit thanks to the reduced switch count is an appealing benefit of string-to-cell equalizers, the existence of a multi-winding transformer [30]–[33] is cited as a top concern because of its design difficulty [41]. The single-switch equalizer [34] is a transformer-less topology, but it is prone to be bulky and costly as the inductor count is proportional to n. Two-switch equalizers [35], [36], on the other hand, require neither a multi-winding transformer nor numerous inductors, hence achieving simplified and miniaturized circuit. Their extendibility or modularity, however, is considered poor because their transformer needs to be redesigned when n is changed.

As mentioned in Section I, integrated converters realize system-level simplification by combining a bidirectional converter and equalizer into a single unit. In addition, conventional integrated converters [37], [38] are also simple because of the two-switch topologies. However, since these integrated converters require a transformer(s), and therefore, the issue of the poor extendibility firmly remains. On the other hand, no transformer is necessary in the proposed integrated converter thanks to the inductor-based voltage divider. Thus, the proposed integrated converter achieves not only simplified system and circuit but also good extendibility. Meanwhile, an equalization speed of the proposed converter is as good as string-to-cell equalizers because the voltage multiplier in the proposed integrated converter is equivalent to a string-to-cell equalizer.

The proposed integrated converter is considered advantageous in terms of cost because of the lack of a transformer and reduced switch count. A transformer is usually the bulkiest and most expensive component in power converters. Each active switch requires a peripheral circuit consisting of a gate driver IC, auxiliary power supply, and several passive components, and therefore, a cost of converters soars with the switch count. Thus, the transformer-less two-switch topology would achieve reduced cost by decreasing the number of relatively expensive components.

The estimated cost of the equalizer in the proposed integrated converter for nine cells is shown in Table II (cost of the PWM converter is not included for fair comparison). The total cost of the prototype's equalizer (see Section V-A) was quoted based on volume purchase from the website of Digi-Key Electronics. The estimated cost is merely $6.78 for nine cells ($0.75/cell) and is even cheaper than passive dissipative equalizers that cost approximately $1.0/cell [44]—battery management ICs containing passive equalization capability, such as bq76PL455 for 16 cells (Texas Instruments) and LTC6802 for 12 cells (Analog Devices), for example, cost $14.67 and $11.92, respectively (it should be noted that these ICs also offer battery monitoring, protection, etc.). Thus, the proposed integrated converter would be advantageous even from a cost perspective in comparison with passive equalizers.

III. Operation Analysis

A. Fundamental Operation

The proposed converter operates very similarly to traditional bidirectional PWM converters, which operate as step-down and step-up converters during charging and discharging modes, respectively. In this section, the detailed operation analysis is performed for the charging mode only to save page length, but the discharging mode can be analyzed similarly.

The key operation waveforms and current flow directions when the voltage of the cell B_m, V_m ($1 \le m \le n$), is the lowest in the string are shown in Figs. 5 and 6, respectively—Fig. 6 corresponds to the case of $m = 1$.

Mode 1 ($T_0 < t < T_1$)*:* The high-side switch Q_H is turned-on, and the low-side diode D_{mL} in the voltage multiplier is conducting. The total voltage across the series-connection of

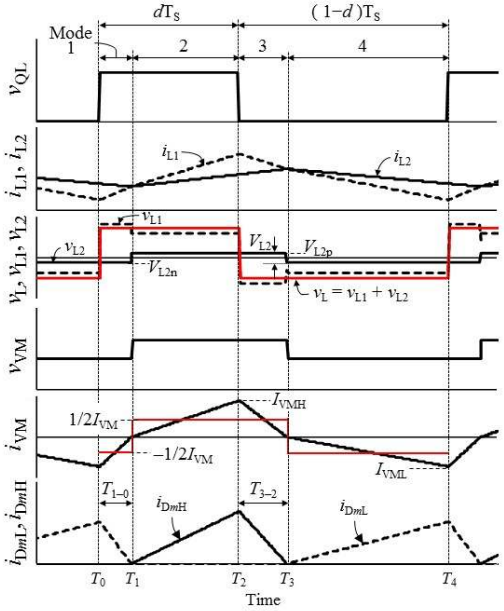


Fig. 5. Operation waveforms during charging when V_m is the lowest in the string.

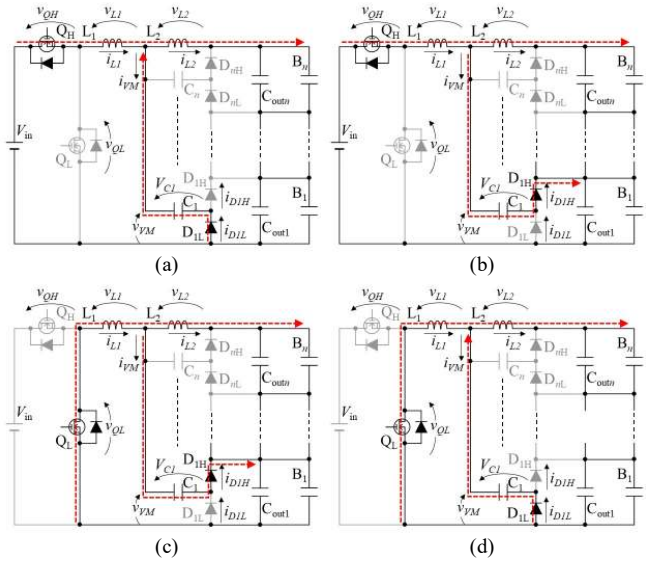


Fig. 6. Operation modes during charging when V_1 is the lowest: (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

L_1 and L_2, v_L, is equal to $V_{in} - V_{st}$ (V_{st} being the string voltage, as designated in Fig. 4). Meanwhile, the current of L_1, i_{L1}, is lower than that of L_2, i_{L2}. The input current of the voltage multiplier i_{VM} is negative because $i_{VM} = i_{L1} - i_{L2}$. The low-side diode D_{mL} conducts when $i_{VM} < 0$, rendering the input voltage of the voltage multiplier v_{VM} at its low level. The voltages of L_1 and L_2, v_{L1} and v_{L2}, are given by

$$\begin{cases} v_{L1} = v_{QL} - v_{VM} \\ v_{L2} = v_{VM} - V_{st} \end{cases}. \quad (1)$$

where v_{QL} is the drain-source voltage of Q_L. Since V_{st} is a fixed value, v_{L2} synchronizes with v_{VM}. Given that the average of v_{L2} is zero under steady-state conditions, v_{L2} becomes negative when v_{VM} is at its low level. v_{L1} is positive because v_{QL} in this mode is equal to V_{in}. Therefore, i_{L1} increases, and i_{L2} decreases.

The input current of the voltage multiplier i_{VM} as well as the current of D_{mL}, i_{DmL}, are equal to the difference between i_{L1} and i_{L2}. From this relationship, i_{VM} in Mode 1 can be yielded as

$$i_{VM-1}(t) = \frac{(L_1 + L_2)(V_{L2} - V_{cm})}{L_1 L_2} t - I_{VML}, \quad (2)$$

where V_{cm} is the voltage of the coupling capacitor C_m, and I_{VML} is the initial value of i_{VM} in Mode 1. As i_{VM} and i_{DmL} reach zero, Mode 1 ends.

Mode 2 ($T_1 < t < T_2$)*:* i_{L1} becomes greater than i_{L2}, and therefore, i_{VM} starts flowing through the high-side diode D_{mH}. The polarity of v_{L2} is reversed as v_{VM} becomes high level, and i_{L2} starts linearly increasing. On the other hand, i_{L1} is still linearly increasing. In addition to the charging current flowing through L_2 to the string, the equalization current coming through D_{mH} is supplied to the least charged cell B_m, as shown in Fig. 6(b).

i_{VM} in Mode 2, i_{VM-2}, is expressed as

$$i_{VM-2}(t) = \frac{(L_1 + L_2)(V_{L2} - V_{cm} - V_{cell})}{L_1 L_2}(t - T_1). \quad (3)$$

Mode 3 ($T_2 < t < T_3$)*:* As the low-side switch Q_L is turned-on, this mode begins. v_{QL} is zero, and the voltage polarity of v_L is reversed as $-V_{st}$, and so does v_{L1} [see (1)]. Meanwhile, i_{VM} is still positive, and therefore v_{VM} is at its high level. From (1), v_{L2} is still positive while v_{L1} becomes negative. Hence, i_{L1} decreases, and i_{L2} increases. D_{mH} is still conducting, and therefore, the equalization current for B_m continues to flow.

i_{VM} in Mode 3, i_{VM-3}, is

$$i_{VM-3}(t) = -\frac{(L_1 + L_2)(V_{cm} + V_{cell})}{L_1 L_2}(t - T_2) + I_{VMH}, \quad (4)$$

where I_{VMH} is the initial current of i_{VM} in Mode 3.

Mode 4 ($T_3 < t < T_4$)*:* Mode 4 begins as the direction of i_{VM} is reversed (i.e., $i_{L1} < i_{L2}$). The polarity of v_{L2} becomes negative as v_{VM} drops, and i_{L2} begins to decrease. i_{L1} is still decreasing because v_{QL} is zero. Hence, both i_{L1} and i_{L2} decrease in this mode.

i_{VM} in Mode 4, i_{VM-4}, is

$$i_{VM-4}(t) = -\frac{(L_1 + L_2)V_{cm}}{L_1 L_2}(t - T_3). \quad (5)$$

Overall, the voltage polarity of v_{L2} is synchronized with i_{VM} as well as i_{DmL} and i_{DmH}. Since the average current of capacitors under steady-state conditions must be zero, the average currents of i_{DmL} and i_{DmH} are equal to the equalization current supplied to B_m. The diodes that are connected in parallel with the cell having the lowest voltage are in operation (i.e., D_{mL} and D_{mH}), whereas others do not conduct. Therefore, similar to conventional voltage equalizers using the voltage multiplier [35], [36], an equalization current is automatically supplied to the least charged cell in the string, and hence, no feedback control loop is necessary for voltage equalization. Thus, controlling the bidirectional PWM converter simply achieves not only charge-discharge cycling but also voltage equalization for series-connected cells.

B. PWM Converter

The operation of the PWM converter in the proposed integrated converter is basically identical to that of the conventional one because the series-connected inductors of L_1 and L_2 can be regarded as a single inductor. As mention in the previous subsection, v_L swings between $V_{in} - V_{st}$ and $-V_{st}$. Therefore, from the volt-second balance on L_1 and L_2, the voltage conversion ratio is yield as

$$V_{st} = dV_{in} \quad (6)$$

where d is the duty cycle of Q_H.

As v_L is divided by two inductors, the peak-to-peak voltage of the square wave voltage to drive the voltage multiplier, V_{L2}, is given by

$$V_{L2} = \frac{L_2}{L_1 + L_2} V_{in}. \quad (7)$$

C. Voltage Multiplier

The operational symmetry between Modes 1–2 and 3–4 yields the relationship between period of Mode 1 and Mode 3, $T_{1-0} = T_1 - T_0$ and $T_{3-2} = T_3 - T_2$ as

$$T_{3-2} = \frac{1-d}{d} T_{1-0}. \quad (8)$$

$i_{VM-1}(T_0)$ is equal to $i_{VM-4}(T_4)$,

$$I_{VML} = \frac{(L_1 + L_2)V_{cm}}{L_1 L_2}(T_s - T_3). \quad (9)$$

From (2), I_{VML} can be expressed as

$$I_{\mathrm{VML}}=\frac{(L_1+L_2)(V_{\mathrm{L2}}-V_{cm})}{L_1L_2}(T_1-T_0)\cdot \tag{10}$$

Considering $T_3 = dT_s + T_{3-2}$, V_{cm} can be obtained from (8), (9), and (10), as

$$V_{cm}=\frac{V_{\mathrm{L2}}}{\frac{(1-d)T_s}{T_{1-0}}+\frac{2d-1}{d}}\cdot \tag{11}$$

From the volt-second balance on L_2, V_{cm} is expressed as

$$V_{cm}=d(V_{\mathrm{L2}}-V_{\mathrm{cell}})+\left(\frac{2d-1}{d}\right)\frac{T_{1-0}}{T_s}V_{\mathrm{cell}}\cdot \tag{12}$$

From (11) and (12), T_{1-0} can be yielded [see (21) in Appendix].

i_{VM} is rectified in the voltage multiplier and supplied to the least charged cell as a dc current. The rectified i_{VM}, I_{VM}, can be obtained by integrating $|i_{\mathrm{VM}}(t)|$ as

$$\begin{aligned}I_{\mathrm{VM}}&=\frac{1}{2T_s}\int_0^{T_s}\left|i_{\mathrm{VM}}(t)\right|dt\\&=\frac{(1-d)(dT_s-T_{1-0})\left(dT_s-\frac{2d-1}{d}T_{1-0}\right)(L_1+L_2)}{2T_sL_1L_2}(V_{\mathrm{L2}}-V_{\mathrm{cell}})\end{aligned}\cdot \tag{13}$$

This equation implies that I_{VM} declines slightly with V_{cell}. When V_{cell} can be assumed small enough compared to V_{L2}, (13) can be rewritten as

$$I_{\mathrm{VM}}=\frac{(1-d)(dT_s-T_{1-0})\left(dT_s-\frac{2d-1}{d}T_{1-0}\right)}{2T_sL_1}V_{\mathrm{in}}\cdot \tag{14}$$

The equation suggests that even if a voltage of the least charged cell is zero, I_{VM} can automatically be limited within a desired value because I_{VM} of (14) is independent on cell voltage. Thus, no feedback control for equalization current limitation is necessary in the proposed integrated converter.

D. Equalization Mechanism

The equalization mechanism of the voltage multiplier can be intuitively understood with an equivalent circuit shown in Fig. 7. As shown in Fig. 5, the ac voltage of v_{L2} (i.e., square wave voltage) is generated across L_2, and capacitors C_1–C_n are tied to the ac voltage source of v_{L2}. Hence, these capacitors behave as ac coupling capacitors that allow ac components only to flow through. Based on ac coupling principle, B_1–B_n as well as corresponding doubler circuits (e.g., C_n, D_nL, and D_nH) can be equivalently separated and grounded, although they are at different dc voltage levels, as depicted in Fig. 7. Since all cells as well as corresponding doubler circuits are connected in parallel in this equivalent circuit, the least charged cell having the lowest voltage preferentially receives a current from the voltage multiplier, eventually unifying all cell voltages.

More detailed equalization mechanism can be explained with a dc equivalent circuit. The detailed analysis performed in the previous works [35], [36] proves that all cells in the voltage multiplier are equivalently connected in parallel, deriving the dc equivalent circuit. The dc equivalent circuit of the voltage multiplier in the proposed converter is identical to that presented in [35], [36], as shown in Fig. 8. According to this equivalent circuit, all cells are parallel-connected, and therefore, the cells sequentially receive an equalization current I_{eq} from V_{L2} in the order of cell voltage. In the following, an equivalent resistance is derived.

The derivation is performed for the case shown in Fig. 6, in which V_1 is the lowest in the string. The voltage of C_1 in each operation mode, V_{C1-1}–V_{C1-4}, are expressed as

$$\begin{cases}V_{C1-1}=V_{C1-4}=-V_{\mathrm{L2n}}+V_{\mathrm{st}}+V_{\mathrm{D}}+\frac{1}{2}I_{\mathrm{VM}}r\\V_{C1-2}=V_{C1-3}=V_{\mathrm{L2p}}+V_{\mathrm{st}}-V_1-V_{\mathrm{D}}-\frac{1}{2}I_{\mathrm{VM}}r\end{cases} \tag{15}$$

where r is the collective resistance of the current path in the voltage multiplier, V_{L2p} and V_{L2n} are high- and low-levels of V_{L2}, respectively, and V_{D} is the forward voltage drop of the diodes in the voltage multiplier. The voltage variation of C_1 over a single switching cycle, ΔV_{C1}, can be yielded from (15), as

$$\begin{aligned}\Delta V_{\mathrm{C1}}&=-2V_{C1-1}+2V_{C1-2}\\&=2\left(V_{\mathrm{L2p}}+V_{\mathrm{L2n}}\right)-2V_1-4V_{\mathrm{D}}-2I_{\mathrm{VM}}r\end{aligned}\cdot \tag{16}$$

Considering I_{VM} rectified in the voltage multiplier, ΔV_{C1} can be expressed differently as

$$\Delta V_{\mathrm{C1}}=\frac{1}{2}\frac{I_{\mathrm{VM}}}{C_1f_s}, \tag{17}$$

where f_S is the switching frequency and C_1 is the capacitance of C_1. From (16) and (17),

$$\left(V_{\mathrm{Lp}}+V_{\mathrm{Ln}}\right)=V_{\mathrm{L2}}=2V_{\mathrm{D}}+\frac{I_{\mathrm{VM}}}{2}R_{\mathrm{eq1}}+V_1, \tag{18}$$

where R_{eq1} is

$$R_{\mathrm{eq1}}=\frac{1}{2C_1f_s}+2r\cdot \tag{19}$$

In this section, R_{eq} has been derived only for B_1, but R_{eq} for other cells can be obtained identically.

According to the dc equivalent circuit, equalization currents I_{eq1}–I_{eqn} are distributed depending on cell voltages V_1–V_n and voltage drops across the equivalent resistors R_{eq1}–R_{eqn}. Equalization currents fundamentally tend to flow toward the least charged cell having the lowest voltage. However, the dc equivalent circuit implies that equalization currents would flow toward non-least charged cells if a voltage drop across the equivalent resistor for the least charged cell is large enough to

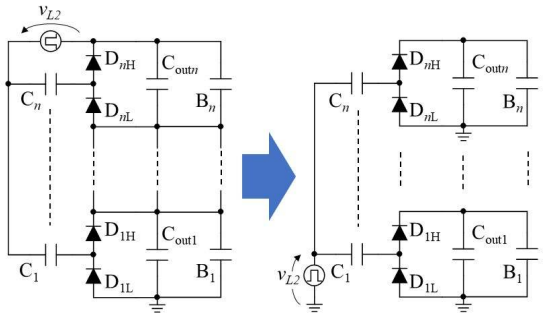


Fig. 7. Equivalent circuit of voltage multiplier.

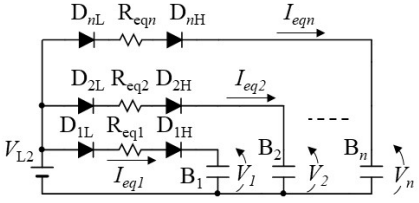


Fig. 8. DC equivalent circuit of voltage multiplier.

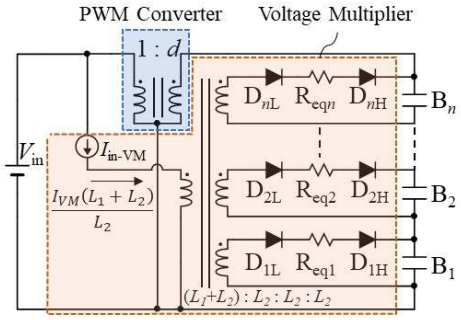


Fig. 9. DC equivalent circuit of proposed converter.

bias diodes for other cells. Hence, in order for the least charged cell only to receive an equalization current from the voltage multiplier, the value of R_{eq} should be designed to be low enough with considering a voltage drop across the equivalent resistor.

E. Operation Criterion

As can be intuitively understood with Fig. 7, in order for equalization currents I_{eq1}–I_{eqn} to flow toward cells, V_{L2} must be higher than the sum of the forward voltage drop of two diodes, voltage drop across R_{eq}, and V_{cell}. It yields the operation criterion of the voltage multiplier from (7);

$$\frac{L_2}{L_1+L_2} > \frac{d}{n} + \frac{2V_D}{V_{in}}. \tag{20}$$

As long as (20) is satisfied, the equalization currents are always supplied to cells, regardless of cell voltage conditions. The larger the value of V_{L2}, the larger will be the equalization current. In other words, the equalization process can be accelerated by increasing the inductance ratio of $L_2/(L_1+L_2)$.

IV. DC Equivalent Circuit of Proposed Integrated Converter

As mentioned in Section II-A, the proposed converter is basically the combination of the PWM converter and the voltage multiplier. A dc equivalent circuit of the proposed integrated converter can also be derived from the combination of the equivalent circuits of the PWM converter and voltage multiplier (see Fig. 8), as shown in Fig. 9. The transformers used in the dc equivalent circuit are ideal transformers and their turn ratios are 1 : d and L_1+L_2 : L_2 : … : L_2. The primary winding of the ideal multi-winding transformer is connected to the PWM converter's input through a current source of $I_{in–VM}$ in order to extract the current of $I_{VM}(L_1+L_2)/L_2$.

Since the dc equivalent circuit contains no high-frequency switching device, the simulation time and burden can be dramatically reduced compared to those for the original circuit-based simulation analysis. Thus, the derived dc equivalent circuit would be a useful tool to efficiently investigate equalization characteristics and influence of the parameter mismatching originating from component tolerance. The simulation results of charge-discharge cycling tests using the derived dc equivalent circuit will be shown in Section V-F.

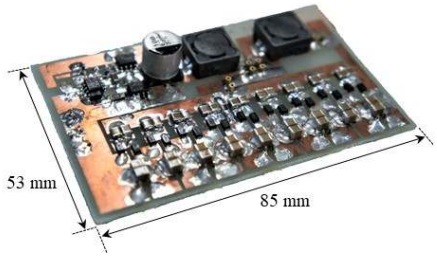


Fig. 10. Photograph of 25-W prototype of transformer-less integrated converter for nine cells connected in series.

Table III Component values.

	Component	Value
Bidirectional Converter	C_{in}	Aluminum Electrolytic Capacitor, 100 µF
	Q_H, Q_L	N-Ch MOSFET, FDS86240, R_{on} = 19.8 mΩ
	L_1	100 µH, 220 mΩ
	L_2	100 µH, 220 mΩ
Voltage Multiplier	C_1–C_9	Ceramic Capacitor, 22 µF
	C_{out1}–C_{out9}	Ceramic Capacitor, 100 µF × 2
	D_1–D_{18}	Schottky Diode, PMEG1030EH, V_D = 0.20 V, R_D = 62.8 mΩ

V. Experimental Result

A. Prototype and Experimental Setup

The 25-W prototype of the proposed transformer-less integrated converter for nine cells connected in series was built, as shown in Fig. 10. The component values used for the prototype are listed in Table III. C_{in} and C_{out1}–C_{out9} denote smoothing capacitors, which were connected in parallel to the input port and each cell.

In general, an equalization current that is hundred times smaller than a charging/discharging current is considered practical to eliminate voltage imbalance [42], [43]. However, in order to expedite the equalization in the experiment, the inductance of L_1 and L_2 were determined to be 100 µH so as to increase the average equalization current as high as approximately 150 mA at d = 0.5, while the experimental charging/discharging current was around 1.0 A (see Section V-D). The prototype was operated at a fixed switching frequency f_s = 100 kHz and the input voltage V_{in} = 48 V for the characteristic measurement tests.

B. Characteristic of Voltage Multiplier

The proposed integrated converter operates either in voltage-balanced or -imbalanced conditions, depending on cell voltage conditions. To investigate the individual characteristic of the voltage multiplier, the experimental setup shown in Fig. 11 was

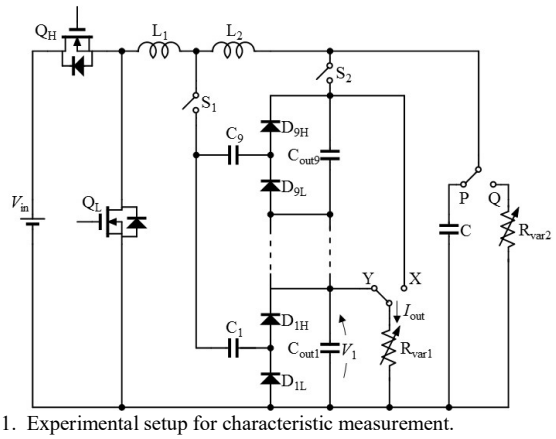
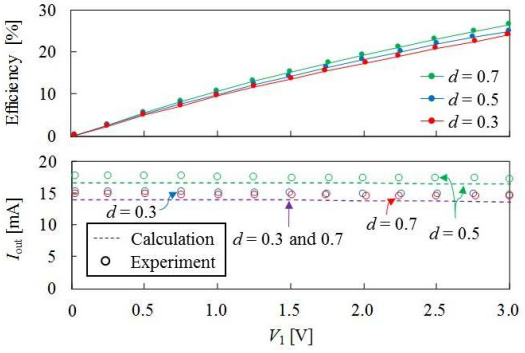
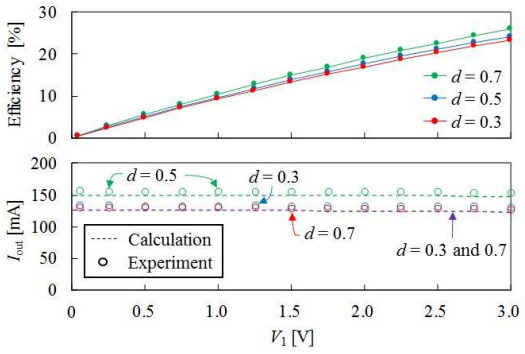


Fig. 11. Experimental setup for characteristic measurement.



(a)



(b)

Fig. 12. Measured characteristics of voltage multiplier under (a) voltage balanced and (b) voltage-imbalanced conditions.

used. The voltage multiplier was enabled by closing the switch S_1, and the variable resistor R_{var2} was removed by selecting the tap P. Current flow directions under the voltage-balanced and -imbalanced conditions were emulated by selecting the intermediate tap X and Y, respectively.

The measured power conversion efficiencies and output current characteristics at d = 0.3, 0.5, and 0.7 are shown in Fig. 12. The theoretical characteristics of (13) are also plotted. In both conditions, the measured current characteristics were in good agreement with the theoretical ones.

The measured efficiencies monotonically increased with V_1. The efficiencies under the voltage-balanced condition were slightly higher than those under the voltage-imbalanced condition. This slight gap is attributable to the current concentration to the least charged cell under the voltage-imbalanced condition; equalization currents under the balanced condition flow toward all cells, hence mitigating Joule losses in the voltage multiplier. Since the diode voltage drop occupies a significant portion of the cell voltage in practical use, the efficiency of the voltage equalizer tends to be low.

Measured power conversion efficiencies of the voltage multiplier in the integrated converter (< 30%) were rather lower than those of the conventional equalizer (60–70%) [35]. The dominant factor of the worse efficiencies was attributable to relatively large ESRs of L_1 and L_2 (see Table III). In the proposed integrated converter, the PWM converter and voltage multiplier share these inductors, and the former processes much larger power. Therefore, the inductors were selected with mainly focusing on the PWM converter, not the voltage multiplier—the inductors were designed so that the ripple currents of i_{L1} and i_{L2} be approximately 30%. In other words,

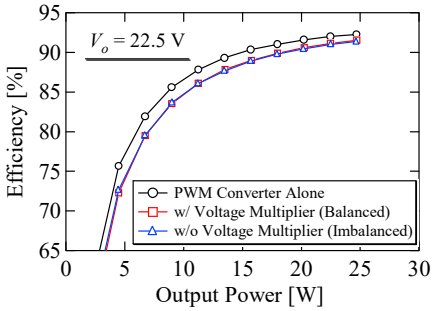


Fig. 13. Measured power conversion efficiencies of integrated converter.

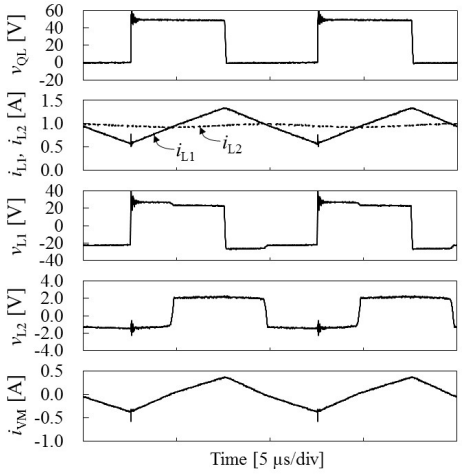


Fig. 14. Measured operation waveforms during charging.

these inductors were not optimized for the voltage multiplier. This is the disadvantage of the integrated converters, as discussed in Section II-B. Nevertheless, this poor efficiency performance would be acceptable in many applications because processed power in the equalizer is far smaller than that of the PWM converter, as mentioned in Section V-A, and the loss in the voltage multiplier would be negligible—in general, an equalization current necessary is less than one-hundredth of the string current [42], [43].

C. Power Conversion Efficiency

Power conversion efficiencies of the PWM converter alone (i.e., without the voltage multiplier) were measured closing Q in Fig. 11, while the voltage multiplier was removed by opening S_1. For comparison, efficiencies of the integrated converter as a whole (i.e., with the voltage multiplier) were also measured with closing both S_1, S_2, and Q.

Measured efficiencies are shown and compared in Fig. 13. The efficiencies of the integrated converter as a whole were slightly lower than those of the PWM converter alone. Efficiency gaps were due to the inefficient voltage multiplier, as can be seen in Fig. 12. These gaps became insignificant as the output power increased. This tendency indicated that the losses associated with the voltage multiplier took only a small portion of the total output power in heavy load region. Given that an equalization current in practical use is less than one-hundredth of charge/discharge currents [42], [43], losses of the voltage multiplier would be negligibly small. Meanwhile, the

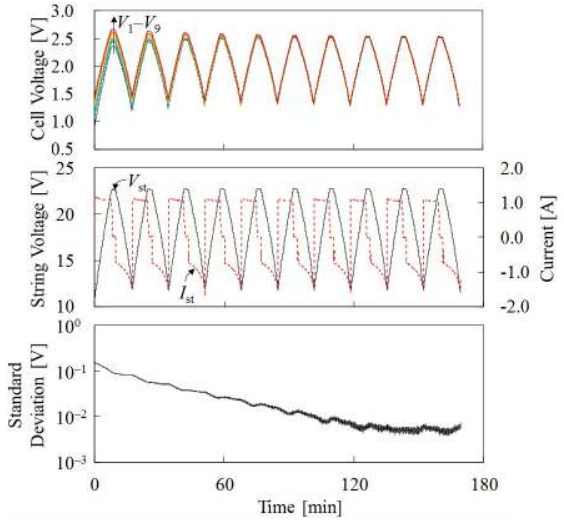


Fig. 15. Resultant charge-discharge cycling profiles.

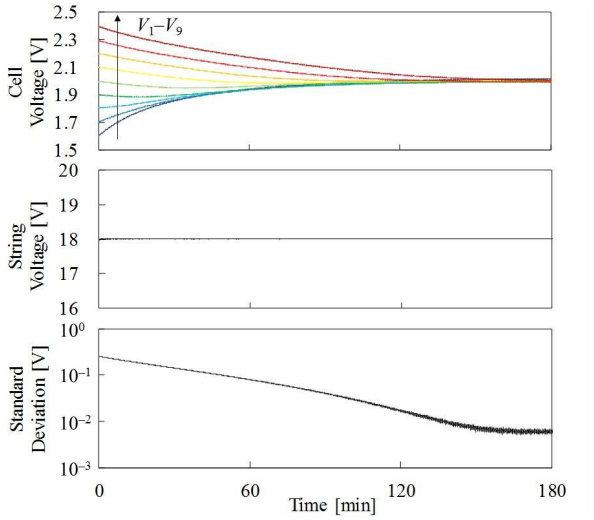


Fig. 16. Resultant voltage equalization profiles during rest time.

integrated converter under the voltage-balanced and -imbalanced conditions exhibited nearly identical efficiency characteristics. This is because efficiencies of the voltage multiplier alone were almost independent on whether cell voltages were balanced, as can be seen in Fig. 12.

D. Equalization Test during Charge-Discharge Cycling

To verify the efficacy of the proposed integrated converter, the equalization test during the charge-discharge cycling was performed from a voltage-imbalanced condition. Nine EDLCs, each with a capacitance of 400 F at a rated voltage of 2.5 V, were used and their initial voltages were imbalanced within the range of 0.90–1.45 V. Each cycle consisted of a constant current–constant voltage (CC–CV) charging of 1.0 A–22.5 V (2.5 V/cell) and 15-W constant-power discharging. TMS320F28335 control card (Texas Instruments) was used for the charge-discharge regulation.

The measured operation waveforms during charging are shown in Fig. 14. The measured waveforms agreed very well with the theoretical ones shown in Fig. 5, verifying the operation of the proposed integrated converter.

The resultant charge-discharge cycling profiles are shown in Fig. 15. The least charged cell B_1 in the string preferentially received the equalization current at the beginning of the cycling, and the voltage imbalance was gradually eliminated as the cycling progressed. The voltage imbalance was eventually eliminated at the end of the experiment, and the standard deviation of cell voltages decreased down to approximately 5.5 mV, demonstrating the equalization performance of the proposed integrated converter.

E. Equalization Test during Rest Time

The equalization test during battery rest time was also performed from an initially-voltage-imbalanced condition—cell voltages were imbalanced within 1.6–2.4 V. In order to emulate the rest time operation, the duty cycle d of the prototype was fixed so that the integrated converter operated in CV charging of 18 V with nearly 0 A.

The measured equalization profiles are shown in Fig. 16. Cells with low initial voltages received equalization currents, and their voltages increased. Meanwhile, other cell voltages declined as their energies were taken away and were transferred to low voltage cells via the integrated converter. In other words, energies of the cells with high initial voltages were redistributed to cells with low initial voltages. All the cell voltages gradually converged, and the voltage imbalance eventually disappeared. The standard deviation of cell voltages was as low as 6.0 mV at the end of the experiment.

F. Simulation Verification

The charge-discharge cycling based on the derived dc equivalent circuit shown in Fig. 9 was also performed under the same condition as the experiment. Capacitors with 400 F capacitance were used as cells, and R_{eq} was determined to be 820 mΩ based on (19). I_{in_VM} in Fig. 9 was programmed to obey (13).

The simulation results are shown in Fig. 17. Similar to the experimental results of charge-discharge cycling, the voltage imbalance was gradually eliminated as time elapsed. In the first

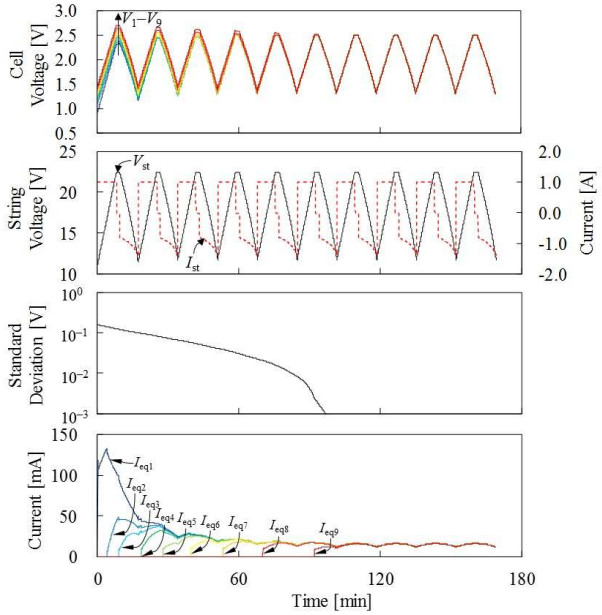


Fig. 17. Simulation charge–discharge cycling profiles.

cycle, the equalization current was preferentially supplied to the least charged cell B_1, and the standard deviation gradually decreased. Equalization currents I_{eq2}–I_{eq9} began to flow sequentially as each voltage became the lowest in the string—under the condition of $V_1 = V_2 = V_3 < V_4$–V_9, for example, B_1–B_3 correspond to the least charged cell in the string. In the 7th cycle, all the cell voltages were unified, so were all the equalization currents I_{eq1}–I_{eq9}. Since all the capacitors were ideal having the identical capacitance in the simulation analysis, voltage imbalance due to the capacitance mismatch never occurred. Hence, the standard deviation in the simulation dropped even below 1 mV, whereas that in the experiment decreased as low as 5.5 mV due to the slight capacitance mismatch. Overall, the simulation result was in good agreement with the experiment shown in Fig. 15, verifying the derived dc equivalent circuit.

VI. Conclusions

The transformer-less bidirectional PWM converter integrating cell voltage equalizer has been proposed in this paper. The proposed integrated converter basically consists of the bidirectional PWM converter and the voltage multiplier. The inductor-based voltage divider is employed to produce a square wave voltage having an arbitrary peak-to-peak voltage, by which the voltage multiplier is driven. Since the PWM converter and voltage equalizer can be integrated into a single unit without introducing a transformer, not only are the system- and circuit-level simplifications feasible but also the design flexibility and extendibility can be improved compared to the conventional integrated converters.

The detailed operational analysis was performed, and the equalization current model was mathematically obtained. The obtained current model suggested that the equalization current can be limited under a desired value even if some cell voltages are zero.

The charge-discharge cycling test using the prototype from the voltage-imbalanced condition was performed for nine EDLCs connected in series. The voltage imbalance was gradually eliminated as the charge-discharge cycling progressed, and all the cell voltages were eventually unified at the end of the experiment, demonstrating the efficacy of the proposed integrated converter.

References

[1] M. Uno and K. Tanaka, "Accelerated charge-discharge cycling test and cycle life prediction model for supercapacitors in alternative battery applications," *IEEE Trans. Ind. Electron*., vol. 59, no. 12, pp. 4704–4712, Dec. 2012.

[2] M. Uno and A. Kukita, "Cycle life evaluation based on accelerated aging testing for lithium-ion capacitors as alternative to rechargeable batteries," *IEEE Trans. Ind. Electron*., vol. 63, no. 3, pp. 1607–1617, Mar. 2016.

[3] J.G. Lozano, E.R. Cadaval, M.I.M. Montero, M.A.G. Martinez, "Battery equalization active methods," *J. Power Sources*, vol. 246, pp. 934–949, Jan. 2014.

[4] P.A. Cassani and S.S. Williamson, "Feasibility analysis of a novel cell equalizer topology for plug-in hybrid electric vehicle energy-storage systems," *IEEE Trans. Veh. Technol*., vol. 58, no. 8, Oct. 2009, pp. 3938–3946.

[5] T. H. Phung, A. Collet, and J. Crebier, "An optimized topology for next-to-next balancing of series-connected lithium-ion cells," *IEEE Trans. Power Electron*., vol. 29, no. 9, Sep. 2014, pp. 4603–4613.

[6] K. Nishijima, H. Sakamoto, and K. Harada, "A PWM controlled simple and high performance battery balancing system," in Proc. *IEEE Power Electron. Spec. Conf*., pp. 517–520, Jun. 2000.

[7] Y. S. Lee and M. W. Cheng, "Intelligent control battery equalization for series connected lithium-ion battery strings," *IEEE Trans. Ind. Electron*., vol. 52, no. 5, pp. 1297–1307, Oct. 2005.

[8] Y. S. Lee, M. W. Cheng, S. C. Yang, and C. L. Hsu, "Individual cell equalization for series connected lithium-ion batteries," *IEICE Trans. Commun*., vol. E89-B, no. 9, pp. 2596–2607, Sep. 2006.

[9] C. S. Moo, Y. C. Hsieh, and I. S. Tsai, "Charge equalization for series-connected batteries," *IEEE Trans. Aerosp. Electron. Syst*., vol. 39, no. 2, pp. 704–710, Apr. 2003.

[10] Y. S. Lee, and G. T. Cheng, "Quasi-resonant zero-current-switching bidirectional converter for battery equalization applications," *IEEE. Trans. Power Electron*., vol. 21, no. 5, pp. 1213–1224, Sep. 2006.

[11] F. Mestrallet, L. Kerachev, J. Crebier, and A. Collet, "Multiphase interleaved converters for lithium battery active balancing," *IEEE Trans. Power Electron*., vol. 29, no. 6, pp. 2874–2881, Jun. 2014.

[12] Y. Shang, Q. Zhang, N. Cui, and C. Zhang, "A cell-to-cell equalizer based on three-resonant-state switched-capacitor converter for series-connected battery strings," *Energies*., vol.10, no. 206, 2017.

[13] A. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Trans. Ind. Appl*., vol. 55, no. 6, Jun. 2008, pp. 2277–2285.

[14] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," in Proc. *IEEE Appl. Power Electron. Conf. Expo*., pp. 848–854, Feb. 1997.

[15] M. Y. Kim, C. H. Kim, J. H. Kim, and G. W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3989–3999, Aug. 2014.

[16] R. Lu, C. Zhu, L. Tian, and Q. Wang, "Super-capacitor stacks management system with dynamic equalization techniques," *IEEE Trans. Magnetics*, vol. 43, no. 1, pp. 254–258, Jan. 2007.

[17] M. Uno and K. Tanaka, "Influence of high-frequency charge-discharge cycling induced by cell voltage equalizers on the life performance of lithium-ion cells," *IEEE Trans. Veh. Technol*., vol. 60, no. 4, May 2011, pp. 1505–1515.

[18] M. Uno and H. Toyota, "Supercapacitor-based energy storage system with voltage equalizers and selective taps," in Proc. *IEEE Power Electron. Specialist Conf*., pp. 755–760, Jun. 2008.

[19] M. Uno and H. Toyota, "Equalization technique utilizing series-parallel connected supercapacitors for energy storage system," in Proc. *IEEE Int. Conf. Sustainable Energy*, pp. 999–1003, Nov. 2008.

[20] H. S. Park, C. H. Kim, K. B. Park, G. W. Moon, and J. H. Lee, "Design of a charge equalizer based on battery modularization," *IEEE Trans. Veh. Technol*., vol. 58, pp. 3216–3223, Sep. 2009.

[21] Y. Yuanmao, K. W. E. Cheng, and Y. P. B. Yeung, "Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string," *IEEE Trans. Power Electron*., vol. 27, no. 7, pp. 3234–3242, Jul. 2012.

[22] M. A. Hannan, M. M. Hoque, S. E. Peng, and M. N. Uddin, "Lithium-ion battery charge equalization algorithm for electric vehicle applications", *IEEE Trans. Ind. Appl*., vol. 53, no. 3, pp. 2541–2549., May/Jun. 2008.

Appendix

$$T_{1-0} = \frac{-\left\{\frac{(1-d)(2d-1)}{d}V_{cell} + (2d-1)(V_{L2}-V_{cell})\right\} - \sqrt{\left\{\frac{(1-d)(2d-1)}{d}V_{cell} + (2d-1)(V_{L2}-V_{cell}) - V_{L2}\right\}^2 - 4\frac{(2d-1)^2}{d}V_{cell}(1-d)(V_{L2}-V_{cell})}}{2\left(\frac{2d-1}{d}\right)^2 \frac{V_{cell}}{T_s}} \quad (21)$$

[23] K. M. Lee, Y. C. Chung, C. H. Sung, and B. Kang, "Active cell balancing of Li-ion batteries using LC series resonant circuit," *IEEE Trans. Ind. Electron*., vol. 62, no. 9, pp. 5491–5501, Sep. 2015.
[24] Y. Shang, C. Zhang, N. Cui, and J. M. Guerrero, "A cell-to-cell battery equalizer with zero-current switching and zero-voltage gap based on quasi-resonant LC converter and boost converter," *IEEE Trans. Power Electron*., vol. 30, no. 7, pp. 3731–3747, Jul. 2015.
[25] S. Yarlagadda, T. T. Hartley, and I. Husain, "A battery management system using an active charge equalization technique based on a dc/dc converter topology," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2720–2729, Nov./Dec. 2013.
[26] F. Baronti, G. Fantechi, R. Roncella, and R. Saletti, "High-efficiency digitally controlled charge equalizer for series-connected cells based on switching converter and upper-capacitor," *IEEE Trans*. *Ind*. *Inform*., vol. 9, no. 2, pp. 1139–1147, May 2013.
[27] C. H. Kim, M. Y. Kim, H. S. Park, and G.W. Moon, "A modularized two-stage charge equalizer with cell selection switches for series-connected lithium-ion battery string in a HEV," *IEEE Trans*. *Power Electron*., vol. 27, no. 8, pp. 3764–3774, Aug. 2012.
[28] C. H. Kim, M. Y. Kim, and G. W. Moon, "A modularized charge equalizer using a battery monitoring IC for series-connected Li-ion battery strings in electric vehicles," *IEEE Trans. Power Electron*., vol. 28, no. 8, pp. 3779–3787, Aug. 2013.
[29] A. M. Imtiaz, F. H. Khan, and H. Kamath, "Time shared flyback converter" based regenerative cell balancing technique for series connected Li-ion battery strings," *IEEE Trans. Power Electron*., vol. 28, no. 12, pp. 5960–5975, Dec. 2013.
[30] T. Anno and H. Koizumi, "Double-input bidirectional dc/dc converter using cell-voltage equalizer with flyback transformer," *IEEE Trans. Power Electron*., vol. 30, no. 6, pp. 2923–2934, Jun. 2015.
[31] N. H. Kutkut, D. M. Divan, and D. W. Novotny, "Charge equalization for series connected battery strings," *IEEE Trans. Ind. Appl*., vol. 31, no. 3, pp. 562–568, May/Jun. 1995.
[32] A. Xu, S. Xie, and X. Liu, "Dynamic voltage equalization for series-connected ultracapacitors in EV/HEV applications," *IEEE Trans. Veh. Technol*., vol. 58, no. 8, pp. 3981–3987, Oct. 2009.
[33] L. Li, Z. Huang, H. Li, and H. Lu, "A high-efficiency voltage equalization scheme for supercapacitor energy storage system in renewable generation applications," *Sustainability*, vol. 8, no. 548, Jun. 2016.
[34] M. Uno and K. Tanaka, "Single-switch cell voltage equalizer using multistacked buck–boost converters operating in discontinuous conduction mode for series-connected energy storage cells," *IEEE Trans. Veh. Technol*., vol. 60, no. 8, pp. 3635–3645, Oct. 2011.
[35] M. Uno and K. Tanaka, "Double-switch single-transformer cell voltage equalizer using a half-bridge inverter and voltage multiplier for series-connected supercapacitors," *IEEE Trans. Veh. Technol*., vol. 61, no. 9, pp. 3920–3930, Nov. 2012.
[36] M. Uno and A. Kukita, "Double-switch equalizer using parallel- or series-parallel-resonant inverter and voltage multiplier for series-connected supercapacitors," *IEEE Trans. Power Electron*., vol. 29, no. 2, pp. 812–828, Feb. 2014.
[37] Y. H. Hsieh, T. J. Liang, S. M. Chen, W. Y. Horng, and Y. Y. Chung, "A novel high-efficiency compact-size low-cost balancing method for series-connected battery applications," *IEEE Trans. Power Electron*., vol. 28, no. 12, pp. 5927–5939, Dec. 2013.
[38] M. Uno and A. Kukita, "Bidirectional PWM converter integrating cell voltage equalizer using series-resonant voltage multiplier for series-connected energy storage cell," *IEEE Trans. Power Electron*., vol. 30, no. 6, pp. 3017–3090, Jun. 2015.
[39] M. Uno and A. Kukita, "PWM converter integrating switched capacitor converter and series-resonant voltage multiplier as equalizers for photovoltaic modules and series-connected energy storage cells for exploration rovers," *IEEE Trans. Power Electron*., vol. 32, no. 11, pp. 8500-8513, Nov. 2017.
[40] K. Yashiro and M. Uno, "Transformer-less bidirectional PWM converter integrating cell voltage equalizer using voltage multiplier for series-connected energy storage cells," in Proc. *IEEE Int. Future Energy Electron. Conf. (IFEEC)*, pp. 1322–1327, Jul. 2017.
[41] J. Cao, N. Schofield, and A. Emadi, "Battery balancing methods: A comprehensive review," in Proc. *IEEE Veh. Power Propulsion Conf*., Sep. 2008, pp. 1–6.
[42] J. W. Kimball, B. T. Kuhn, and P. T. Krein, "Increased performance of battery packs by active equalization," in Proc. *IEEE Veh. Power Propulsion Conf*., pp. 323–327, Sep. 2007.
[43] S. West and P. T. Krein, "Equalization of valve-regulated lead-acid batteries: Issues and life test results," in Proc. *Int. Telecommun. Energy Conf*., pp. 439–446, Sep. 2000.
[44] D. Andrea, *Battery Management Systems for Large Lithium-Ion Battery Packs*, Boston: Artech House, 2010, ch.3.2.3.3.

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