Nonisolated PWM Three-Port Converter Realizing Reduced Circuit Volume for Satellite Electrical Power Systems

Hikaru Nagata, and Masatoshi Uno, *Member, IEEE*

***Abstract*— Three-port converters (TPCs) combining two dc-dc converters into a single unit is a promising solution that can simplify and miniaturize satellite electrical power systems. Conventional nonisolated TPCs, however, face a variety of challenges, such as the necessity of a transformer, low effective duty cycle operation, and unshared ground issues. This paper proposes a novel nonisolated TPC integrating a unidirectional and bidirectional PWM converters. The two converters can be integrated into a single unit with reducing total switch count without employing a transformer, achieving the simplified circuit. In addition, thanks to the capacitor added in series with switches, not only is the voltage stress of semiconductor devices reduced but also miniaturized inductor design is feasible. The quantitative analysis revealed that the volume of passive components in the proposed TPC could be reduced by approximately 19% compared to a conventional nonisolated TPC. A 240-W prototype was built for the experimental verification, and the results agreed well with those of the analysis, demonstrating its efficacy.**

***Index Terms*— Satellite electrical power system, PWM converter, regulated bus system, three-port converter.**

H. Nagata is with Hitachi Ltd. Yokohama 244-0817, Japan (e-mail: hikaru.nagata.qw@hitachi.com)

M. Uno is with the Department of Electrical and Electronic Systems Engineering, Hitachi 316-8511, Japan (e-mail: masatoshi.uno.ee@vc.ibaraki.ac.jp).

I. Introduction

Small satellites have been gaining significant attention as they offer frequent mission opportunities at lower costs. Energy requirement significantly varies depending on missions, and therefore, electrical power systems (EPSs) for small satellites are desirably flexible and agile. Traditional satellite power systems can be roughly categorized into two groups: unregulated bus and regulated bus systems, as shown in Figs. 1(a) and (b).

The unregulated bus system, shown in Fig. 1(a), is favorable for relatively low-power satellites (less than a few kilowatts) as its converter count in the power system is only one. A rechargeable battery is directly connected to the bus, and a number of battery cells connected in series is determined by the bus voltage requirement. 28-V and 50-V bus systems, for example, usually require batteries consisting of eight and twelve cells connected in series, respectively. Since the number of battery cells connected in series cannot be arbitrarily changed, an energy of the battery in watt-hour must be adjusted by selecting or manufacturing cells with proper capacity. However, cells with a proper capacity are not often readily available due to limited line-up of space-qualified batteries, and it would be a stumbling block to small satellites to realize frequent mission opportunities.

The regulated bus system, shown in Fig. 1(a), is often employed for large-scale systems, such as communication satellites. A battery is connected to the bus via a bidirectional converter (or charge-discharge regulator), and therefore, the number of cells connected in series can be arbitrary changed to flexibly meet energy requirement. Although the regulated bus architecture is favorable in terms of the design flexibility, the converter count is doubled, hence increasing the system complexity and cost.

Meanwhile, three-port converters (TPCs) integrating two converters into a single unit have been proposed and vigorously developed to achieve simplified systems at a lower cost in renewable power systems and electric vehicles where multiple power sources are installed. The schematic diagram of a power system employing a TPC, shown in Fig. 1(c), incorporates a unidirectional converter with a bidirectional one, hence simplifying the system by halving the converter count.

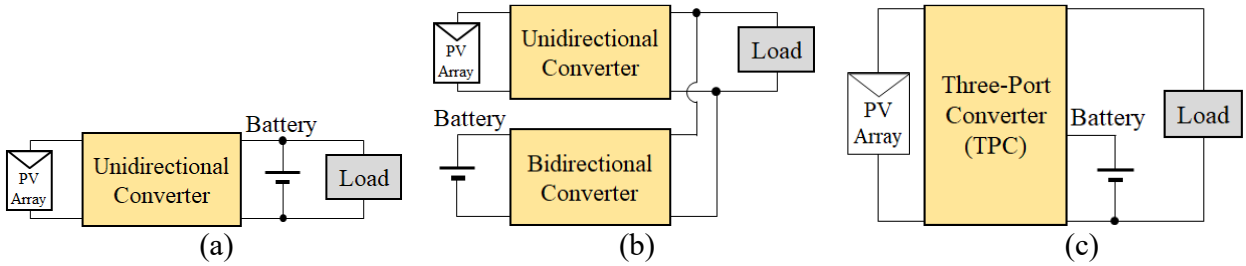


Fig. 1. Schematic diagrams of (a) unregulated bus system, (b) regulated bus system, and (c) regulated bus system with TPC.

TPCs can be roughly categorized into three groups: the isolated, partially-isolated, and nonisolated TPCs. The isolated TPCs are the most straightforward topology that introduces a multi-winding transformer [1]–[5]. Multiple isolated dc-dc converters can be combined based on the magnetic coupling, and all input and output ports are galvanically isolated. Partially-isolated TPCs, on the other hand, are essentially the combination of an isolated and nonisolated dc-dc converters, such as PWM converters [6]–[8], phase-shift converters [9]–[11], and resonant converters [12], [13], reducing the circuit complexity by sharing some circuit elements in the course of the integration. Isolated and partially-isolated TPCs are suitable for applications requiring galvanic isolation, but the existence of the bulky transformer unnecessarily decreases power conversion efficiency and increases the volume and cost in satellite EPSs where galvanic isolation is not mandatory.

Nonisolated TPCs with no transformer are undoubtedly suitable for satellite EPCs. Various kinds of nonisolated TPC topologies have been reported [14]–[24], but some challenges firmly remain. In TPCs operating in a time-division manner, for example, an effective duty cycle for each input port is inevitably shortened because an on-duty cycle in a single switching cycle is shared by multiple input ports. The low effective duty cycle operation increases RMS currents of each input port, and therefore, their power conversion efficiencies naturally tend to deteriorate [14], [15]. Unshared ground issues [16], [17], decreased total power conversion efficiencies due to multiple power conversion stages [18], [19], relatively complex circuits due to large numbers of circuit elements [20]–[24] can also be cited as top concerns.

To address the challenges of the conventional nonisolated TPCs, a novel nonisolated PWM-TPC has been proposed in our previous work [25]. This paper presents the extended and fully-developed work of [25]. The proposed PWM-TPC can operate with high effective duty cycles without suffering from the unshared ground issues. In addition, not only is the circuit very simple but also inductors can be miniaturized thanks to the added capacitor that provides an additional current flow path to a load, as will be discussed in Section III.

The rest of this paper is organized as follows. Key circuit elements to derive the proposed TPC are introduced in Section II. The detailed operation analyses will be performed in Section IV. In Section V, the proposed TPC will be quantitatively compared with a conventional nonisolated TPC [19] and a conventional regulated bus system having two separate converters from the viewpoints of the circuit volume. Experimental results of a 240-W prototype will be presented in Section VI.

II. CIRCUIT ELEMENTS FOR PORPOSED PWM-TPC

A. Key Circuit Elements

The proposed PWM-TPC is derived from the integration of two converters: a unidirectional step-down PWM converter and bidirectional PWM converter, as shown in Figs. 2(a) and (b), respectively. The bidirectional PWM converter is a traditional converter, whereas the unidirectional step-converter is a novel topology. The fundamental operation principle of the unidirectional converter is briefly explained in the following subsection

B. Operation Principle of Unidirectional Step-Down PWM Converter

All circuit elements are assumed ideal, and a diode forward voltage is not taken into account. The voltage of C_a, V_{Ca}, is assumed constant, and its voltage ripple is negligibly small.

The theoretical key operation waveforms and operation modes of the unidirectional step-down converter are shown in Figs. 3 and 4, respectively. Q_{a1} and Q_{a2} are driven in a complementary mode. The duty cycle of Q_{a2} is defined as d. The voltage of C_a, V_{Ca}, is assumed constant, and C_a behaves as a constant voltage source. A forward voltage drop of the diode D_a is neglected.

Mode 1 ($0 < t \leq dT_s$) [Fig. 4(a)]: Q_{a2} is turned-on, and the diode D_a also conducts. C_a is connected in parallel with L_a, and therefore, the voltage applied to L_a in Mode 1, $v_{La.M1}$, and the voltage of C_a, V_{Ca}, are given by

$$v_{La.M1} = V_{Ca} = V_{in} - V_a \tag{1}$$

where V_{in} and V_a are the input and output voltages, respectively. L_a is charged by $V_{in} - V_a$, and its current, i_{La}, linearly increases. C_a is also charged, and its current, i_{Ca}, changes exponentially as it is sandwiched by two voltage sources of V_{in} and V_a. The diode current, i_{Da}, is equal to i_{Ca} in this mode. The voltage applied to Q_{a1} is V_a.

Mode 2 ($dT_s < t \leq T_s$) [Fig. 4(b)]: Q_{a1} and Q_{a2} are turned-on and -off, respectively. L_a and C_a are connected in series and discharged together. The voltage across L_a in Mode 2, $v_{La.M2}$, is

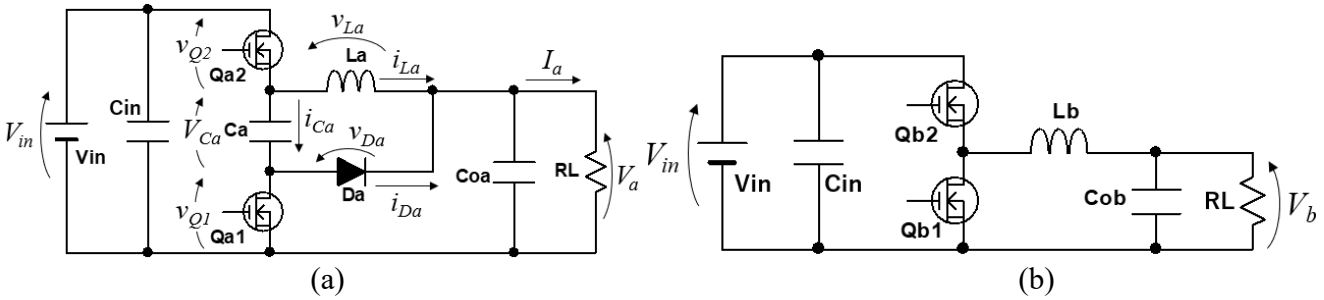


Fig. 2. PWM converters for the proposed TPC: (a) Unidirectional step-down converter (Converter A), (b) bidirectional converter (Converter B).

$$v_{La.M2} = V_{Ca} - V_a = V_{in} - 2V_a \tag{2}$$

The voltage of Q_{a2} is $V_{in} - V_{Ca} = V_a$.

The volt-second balance on L_a with (1) and (2) yields the voltage step-down ratio, as

$$\frac{V_a}{V_{in}} = \frac{1}{2-d} \tag{3}$$

The voltage step-down ratio is dependent on d, and its theoretical conversion range is between 0.5 and 1.0.

The average current of C_a must be zero under steady-state conditions, yielding the following relationship;

$$\int_0^{dT_s} i_{Ca} dt = I_{La}(1-d)T_s \tag{4}$$

where I_{La} is the average current of L_a, and T_s is the switching period. The output current, I_a, is the sum of I_{La} and an average of i_{Da}. Since i_{Da} is equal to i_{Ca} in Mode 1, I_a is expressed as

$$I_a = I_{La} + \frac{1}{T_s}\int_0^{dT_s} i_{Ca} dt = I_{La}(2-d) \tag{5}$$

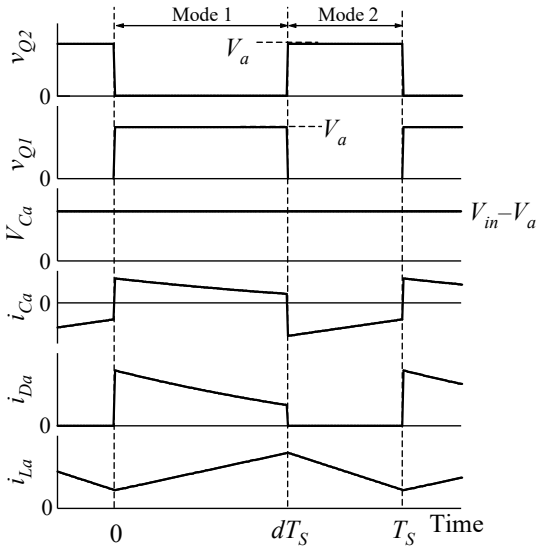


Fig. 3. Key operation waveforms of unidirectional step-down PWM converter.

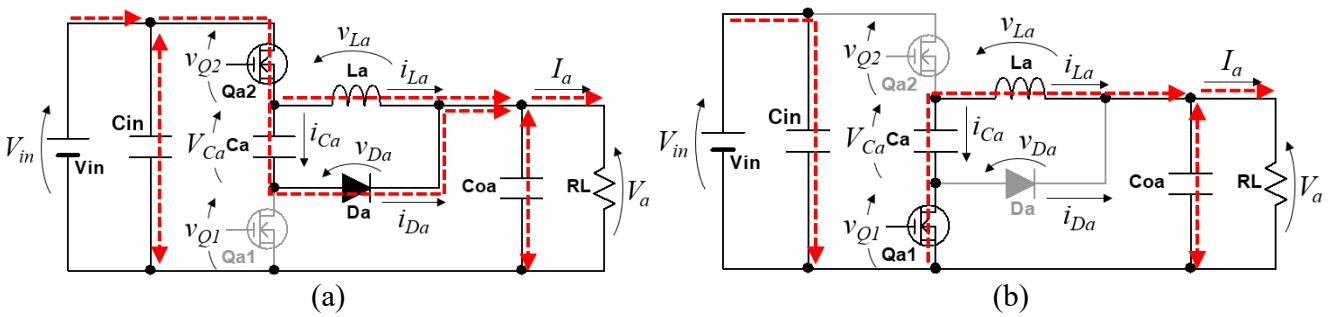


Fig. 4. Operation mode of unidirectional step-down PWM converter: (a) Mode 1, (b) Mode 2.

This equation suggests that the inductor average current I_{La} is smaller than the average output current I_a thanks to C_a carrying a portion of I_a, as can be seen in Fig. 4(a).

An inductor current ripple, ΔI_{La}, is expressed using the ripple current factor $\alpha_L = \Delta I_{La}/I_{La}$, as

$$\Delta I_{La} = \frac{(V_{in} - V_a)dT_s}{L_a} = \frac{(V_a - V_{Ca})(1-d)T_s}{L_a} = \alpha_L I_{La}$$
$$\rightarrow L_a = \frac{(V_{in} - V_a)dT_s}{\alpha_L I_{La}} = \frac{V_a(1-d)T_s}{\alpha_L I_{La}} \quad (6)$$

In general, PWM converters are designed so that α_L is around 0.3.

A capacitor voltage ripple, ΔV_{Ca}, is expressed using the capacitor ripple voltage factor, $\alpha_C = \Delta V_{Ca}/V_{Ca}$, as

$$\Delta V_{Ca} = \frac{I_{La}(1-d)T_s}{C_a} = \alpha_C V_{Ca}$$
$$\rightarrow C_a = \frac{I_{La}(1-d)T_s}{\alpha_C (V_{in} - V_a)} \quad (7)$$

α_C should be so small (less than 0.1) that C_a behaves as a constant voltage source.

III. Proposed Nonisolated PWM-TPC

A. Circuit Derivation

The proposed PWM-TPC is shown in Fig. 5. A startup circuit is used to slowly charge the input smoothing capacitor C_{in} during a startup operation. Converter A, the unidirectional converter, regulates the output voltage V_a. Meanwhile, Converter B, the traditional bidirectional PWM converter, regulates the battery voltage and realizes bidirectional power flow for rechargeable batteries. These two PWM converters are integrated without introducing a transformer nor additional components, and therefore, the proposed

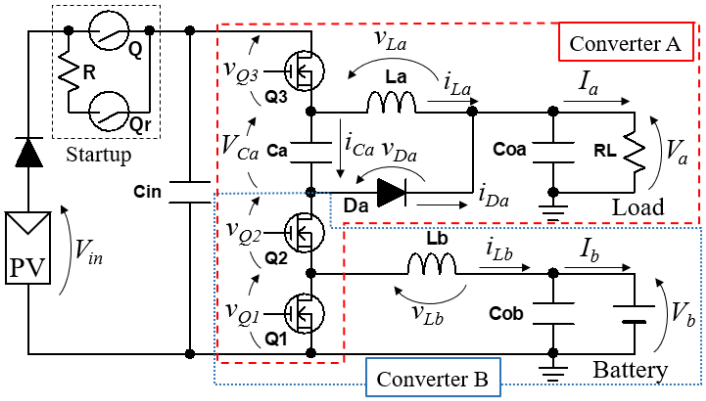


Fig. 5. Proposed nonisolated PWM-TPC.

TPC can be categorized into the nonisolated TPC.

In the proposed TPC, the series connection of Q_1 and Q_2 behaves as Q_{a1} in the unidirectional PWM converter shown in Fig. 2(a). On the other hand, the operation of the series connection of Q_2 and Q_3 in Fig. 5 corresponds to that of Q_{b2} in the bidirectional PWM converter. The output and battery voltages, V_a and V_b, are regulated by adjusting duty cycles of the switches of Q_3 and Q_1, respectively. Two of three switches must be simultaneously on, as will be discussed in Section IV.

B. Benefits and Drawbacks

In comparison with the conventional unregulated bus architecture having two separate converters [Fig. 1(b)], the TPC-based system can be simpler and smaller as two converters are integrated into a single unit with not only sharing switches but also miniaturizing inductors, as will be detailed in Section V. However, the reduced system reliability should be cited as a concern of not only the proposed TPC but also most conventional TPCs—since multiple converters are integrated with sharing circuit elements, one single failure of circuit elements might lead to the failure of the entire converter. The switch Q_2 in the proposed TPC, for instance, is shared by both Converters A and B, and therefore, no power is provided for both the load and battery in case of failure of Q_2. Thus, the simplified and miniaturized circuit of TPCs is a trade-off with reliability. Hence, TPCs are considered suitable for low-power small satellites where reduced complexity, volume, and cost tend to be prioritized over reliability.

In comparison with conventional nonisolated TPCs, the challenges mentioned in Section I can be addressed because the proposed TPC allows high effective duty cycle operation (see Section IV), and all the input and output ports share the same ground.

The capacitor C_a added between Q_2 and Q_3 contributes to reducing the voltage stress of semiconductor devices (switches and a diode D_a). Switches and diodes in conventional PWM converters must be rated for a full input voltage, whereas the voltage stress of semiconductor devices in the proposed TPC is equal to the output voltage V_a, as will be detailed in Section IV. Furthermore, the inductor L_a in Converter A can be miniaturized thanks to C_a that provides an additional current flow path to the load [see Figs. 7(a) and (b)]. In addition, the applied voltages of inductors can be reduced by C_a. The miniaturized circuit design of the proposed TPC will be quantitatively verified in Section V.

The narrower operation region is a drawback of the proposed PWM-TPC. Specifically, allowable duty cycle ranges are dependent on the relationship between the load power P_a and battery charging powers P_b [see (26) and (27)]—P_a must be rather greater than P_b for the TPC to operate. This operational limitation is imposed by the existence of a diode D_a, a unidirectional device, as will be detailed in Section IV-C.

Replacing D_a with a switch, which allows reverse current flow, resolves this operational limitation. However, it increases the circuit complexity to some extent and therefore is not recommended if the circuit simplification is prioritized over extending the operational range.

Given the operational limitation, the proposed TPC is best suitable for applications where batteries are charged slowly with a low charging rate. For example, charging power can be even lower than one-sixth and one-tenth that of discharging or a load power in communication satellites [26] and planetary probes [27].

IV. Operation Analysis

The proposed nonisolated PWM-TPC operates in one of the following three modes: single-input–dual-output (SIDO), single-input–single-output (SISO) and maximum power point tracking (MPPT) modes. In the SIDO mode, the PV array supplies the entire power required by the load and battery charging, and the battery voltage V_b is regulated to be a constant value (i.e., a constant-voltage charging mode). When the PV array produces no power at night, the system operates in the SISO mode, in which the battery alone supplies the entire load power. In the MPPT mode, the PV array operates at its MPP, while the power surplus or deficit is buffered by the battery. This section omits the MPPT mode to save page length as operational waveforms and current flow directions in this mode are essentially identical to those in the SIDO modes.

The following analysis is performed based on the assumption that all circuit elements are ideal, a diode forward voltage is zero, and dead time periods are short enough to be neglected. The voltage of C_a, V_{Ca}, is assumed constant, and its voltage ripple is negligibly small.

A. SIDO Mode

A PV array is capable of supplying the entire load power, and the surplus power is used for battery charging. The key operation waveforms and the current flows in the SIDO mode are shown in Figs. 6 and 7, respectively. d_a and d_b are the on-duty cycle of Q_3 and the off-duty cycle of Q_1, respectively. T_S is the switching period. The startup circuit is not illustrated in Fig. 7 for the sake of clarity.

Mode 1 ($0 < t \le d_b T_s$) [Fig. 7(a)]: D_a, Q_2, and Q_3 are on, and the voltage of Q_1, v_{Q1}, is equal to V_a. Inductor currents, i_{La} and i_{Lb}, linearly increase. The voltages of L_a and L_b, v_{La} and v_{Lb}, are expressed as

$$\begin{cases} v_{La} = V_{in} - V_a \\ v_{Lb} = V_{in} - V_{Ca} - V_b \end{cases} \tag{8}$$

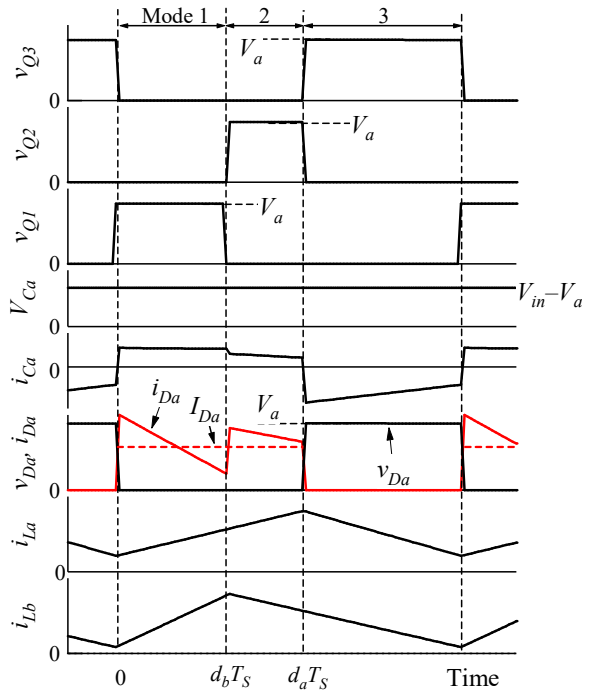


Fig. 6. Key operation waveforms in SIDO mode.

where V_{Ca} is the voltage of C_a. C_a is charged by not only the diode current i_{Da} but also the current of L_b, i_{Lb} (i.e., $i_{Ca} = i_{Da} + i_{Lb}$). In other words, the behaviour of C_a is influenced by both Converters A and B, imposing an operation criterion as will be discussed in Section IV-C.

Mode 2 ($d_bT_s < t \leq d_aT_s$) [Fig. 7(b)]: Q_1 and Q_2 turn off and on, respectively, and the voltage of Q_2, v_{Q2}, rises to V_a. i_{La} still linearly increases, whereas i_{Lb} starts falling. The voltages of L_a and L_b in Mode 2 are given by

$$\begin{cases} v_{La} = V_{in} - V_a \\ v_{Lb} = -V_b \end{cases} \tag{9}$$

In Modes 1 and 2, V_{Ca} is equal to the voltage of L_a, yielding

$$V_{Ca} = V_{in} - V_a \tag{10}$$

Contrary to Mode 1, C_a is charged only by i_{Da} in Mode 2, hence $i_{Ca} = i_{Da}$.

Mode 3 ($d_aT_s < t \leq T_s$) [Fig. 7(c)]: Q_2 and Q_3 are on and off, respectively, and D_a is reverse-biased. The voltage of Q_3 and D_a, v_{Q3} and v_{Da}, are equal to V_a. C_a and L_a are connected in series (i.e., $i_{Ca} = -i_{La}$) and discharge together toward the load. The voltages of L_a and L_b are

$$\begin{cases} v_{La} = V_C - V_a \\ v_{Lb} = -V_b \end{cases} \tag{11}$$

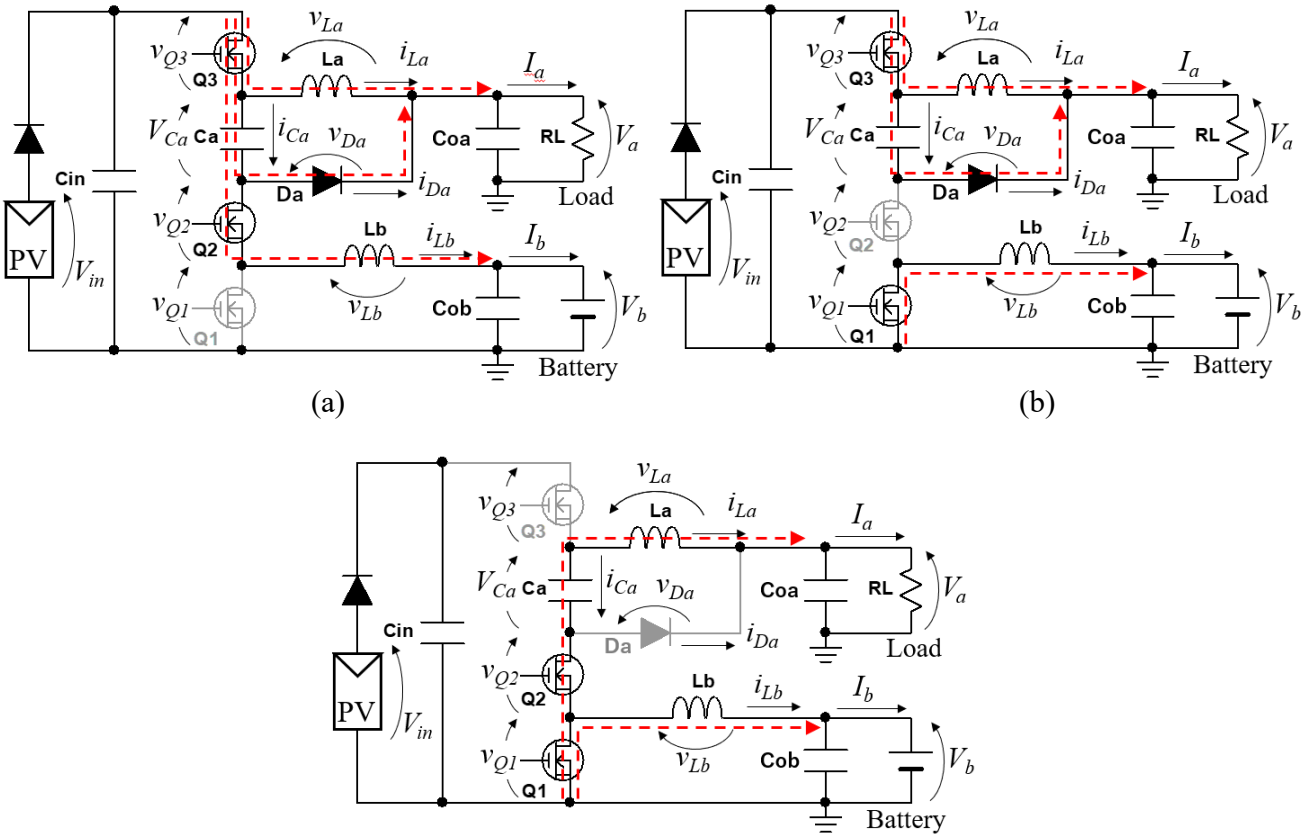


Fig. 7. Current flows in SIDO mode: (a) Mode 1, (b) Mode 2, (c) Mode 3.

In summary, voltages applied to switches and D_a are equal to V_a thanks to C_a, allowing reduced voltage rating of semiconductor devices—switches in traditional PWM buck converters must be rated for the full input voltage V_{in}. Meanwhile, relatively large currents flow through C_a, and therefore a low-ESR capacitor should be employed for C_a to reduce its Joule loss.

From (8)–(11), the volt-second balance on L_a and L_b yields the voltage conversion ratios of M_a and M_b, as

$$M_a = \frac{V_a}{V_{in}} = \frac{1}{2 - d_a} \tag{12}$$

$$M_b = \frac{V_b}{V_{in}} = \frac{d_b}{2 - d_a} \tag{13}$$

The voltage conversion ratio of Converter B (13) is dependent on not only its duty cycle d_b but also d_a, suggesting the interdependence between V_a and V_b. By introducing a decoupling network, the interdependence between V_a and V_b would be satisfactorily eliminated, as reported in [8], [23], which will be a part of our future works.

Current ripples of L_a and L_b, ΔI_{La} and ΔI_{Lb}, are expressed using the ripple current factor α_L, as

$$\Delta I_{La} = \frac{(V_{in} - V_a)d_a T_s}{L_a} = \frac{(V_a - V_{Ca})(1 - d_a)T_s}{L_a} = \alpha_L I_{La}$$
$$\rightarrow L_a = \frac{(V_{in} - V_a)d_a T_s}{\alpha_L I_{La}} = \frac{(V_a - V_{Ca})(1 - d_a)T_s}{\alpha_L I_{La}} \quad (14)$$

$$\Delta I_{Lb} = \frac{(V_{in} - V_{Ca} - V_b)d_b T_s}{L_b} = \frac{V_b(1 - d_b)T_s}{L_b} = \alpha_L I_{Lb}$$
$$\rightarrow L_b = \frac{(V_{in} - V_{Ca} - V_b)d_b T_s}{\alpha_L I_{Lb}} = \frac{V_b(1 - d_b)T_s}{\alpha_L I_{Lb}} \quad (15)$$

The voltage ripple of C_a, ΔV_{Ca}, is expressed using the capacitor ripple factor, $\alpha_C = \Delta V_{Ca}/V_{Ca}$, as

$$\Delta V_{Ca} = \frac{I_{La}(1 - d_a)T_s}{C_a} = \alpha_C V_{Ca}$$
$$\rightarrow C_a = \frac{I_{La}(1 - d_a)T_s}{\alpha_C (V_{in} - V_a)} \quad (16)$$

α_C should be so small (less than 0.1) that C_a behaves as a constant voltage source.

B. SISO Mode

In the SISO mode, Converter B together with D_a composes a PWM boost converter, through which the battery supplies the power to the load. The key operation waveforms and current flows in the SISO mode are shown in Figs. 8 and 9, respectively. Since Converter A, except for D_a, does not participate in the operation of the SISO mode, waveforms and explanations corresponding to Converter A are not presented for the sake of simplicity. Meanwhile, d_a is set to be any value so that C_{in} operates as a clamp capacitor.

Mode 1 ($0 < t \leq (1-d_b)T_s$) [Fig. 9(a)]: Q_1 and Q_2 are on and off, respectively. L_b is charged and its current i_{Lb} linearly changes. The voltage across the inductor L_b in Mode 1 is

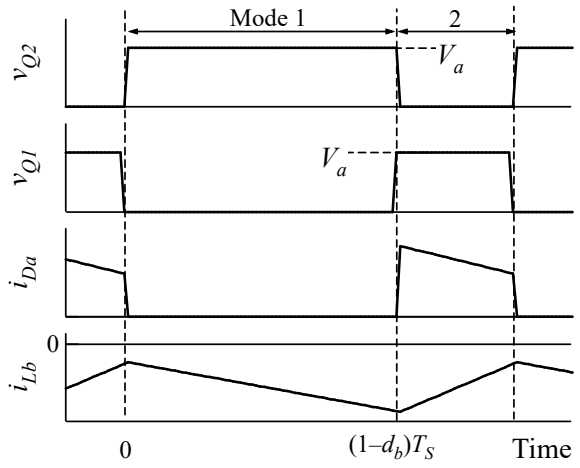


Fig. 8. Key operation waveforms in SISO mode.

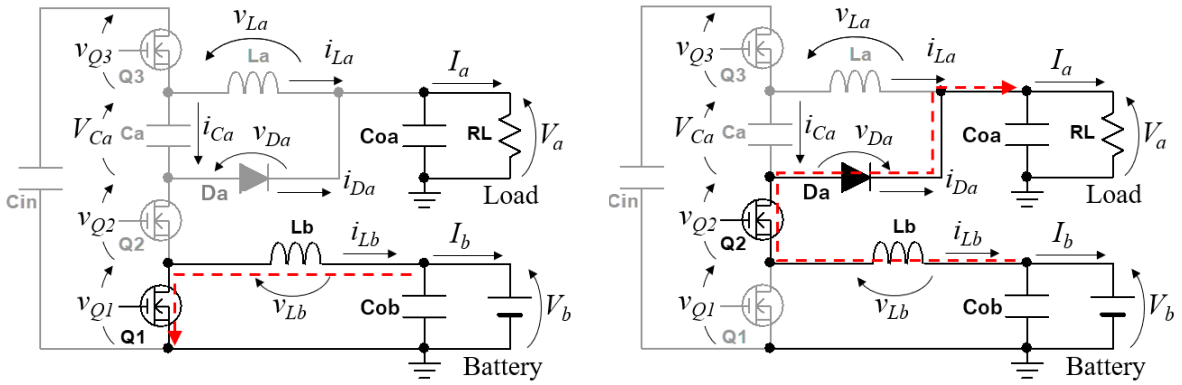


Fig. 9. Current flows in SISO mode: (a) Mode 1, (b) Mode 2.

$$v_{Lb} = -V_b \tag{17}$$

Mode 2 ($(1-d_b)T_s < t \leq T_s$) [Fig. 9(b)]: Gating off Q_1 triggers this mode, and L_b discharges its stored energy through Q_2 and D_a. The voltage of L_b in Mode 2 is

$$v_{Lb} = V_a - V_b \tag{18}$$

The voltage conversion ratio in the SISO mode is determined from the volt-sec balance on L_b, as

$$\frac{V_a}{V_b} = \frac{1}{d_b} \tag{19}$$

In practical operations, Q_3 is recommended to be driven in order for C_{in} to operate as a clamp capacitor—if Q_3 is always off in the SISO mode, a leakage current through Q_3 charges C_{in}, eventually reaching its breakdown voltage. The duty cycle of Q_3 can be arbitrarily set as long as the duty cycle limitation (21), which will be discussed in the next subsection, is satisfied.

In the SISO mode, L_b is charged and discharged whereas L_a and C_a do not take part in the operation. The current ripple of L_b in the SISO mode is given by

$$\Delta I_{Lb} = \frac{(V_a - V_b)d_b T_s}{L_b} = \frac{V_b(1-d_b)T_s}{L_b} = \alpha_L I_{Lb}$$
$$\rightarrow L_b = \frac{(V_a - V_b)d_b T_s}{\alpha_L I_{Lb}} = \frac{V_b(1-d_b)T_s}{\alpha_L I_{Lb}} \tag{20}$$

C. Operation Constraints in SIDO and MPPT Modes

The integration of two PWM converters imposes the two operation constraints in the SIDO and MPPT modes, as discussed below. To properly regulate two output voltages of V_a and V_b independently, these operation constraints need to be satisfied.

In order for Mode 2 to exist, d_a must be greater than d_b because Q_2 together with Q_3 behave as the high-side switch for Converter B. Hence, the duty cycle limitation constraint is given by

$$d_a > d_b \tag{21}$$

Another operation constraint is yielded from the charge balance on C_a. As mentioned in Section III-A, C_a is charged by not only i_{Da} but also i_{Lb}, and is discharged by i_{La}. To simplify the analysis, instantaneous currents of i_{Da}, i_{La} and i_{Lb} are assumed constant as I_{Da}, I_{La} and I_{Lb} (note that I_{Da} is the average current of i_{Da} over Modes 1 and 2, as designated in Fig. 6). i_{Ca} in each mode is expressed as

$$i_{Ca} = \begin{cases} i_{Da} + i_{Lb} \approx I_{Da} + I_{Lb} & (Mode\ 1) \\ i_{Da} \approx I_{Da} & (Mode\ 2) \\ -i_{La} \approx -I_{La} & (Mode\ 3) \end{cases} \tag{22}$$

The charge balance relationship on C_a with (22) yields

$$d_b I_{Lb} + d_a I_{Da} = (1 - d_a) I_{La} \tag{23}$$

The average battery current I_b is equal to I_{Lb} (i.e., $I_b = I_{Lb}$), while the average load current I_a is equal to the sum of I_{La} and $d_a I_{Da}$ (i.e., $I_a = I_{La} + d_a I_{Da}$). By substituting $I_b = I_{Lb}$ and $I_a = I_{La} + d_a I_{Da}$ into (23), I_{La} and I_{Da} can be yielded as

$$I_{La} = \frac{I_a + d_b I_b}{2 - d_a} \tag{24}$$

$$I_{Da} = \frac{I_a(1 - d_a) - d_b I_b}{d_a(2 - d_a)} \tag{25}$$

These equations suggest that the operation of Converter A containing variables of I_{La} and I_{Da} is influenced by Converter B. To ensure the operation shown in Figs. 6 and 7, D_a must conduct, hence $I_{Da} > 0$. Substitution of $I_{Da} > 0$ into (25) yields

$$\frac{I_a}{I_b} > \frac{d_b}{1 - d_a} \tag{26}$$

Eventually, the power balance between the load and battery is determined from the constraint (26). Substituting (12) and (13) into (26) yields the allowable region for the power ratio of P_a/P_b, K, as

$$K = \frac{P_a}{P_b} > \frac{1}{1 - d_a} \tag{27}$$

This equation suggests that the larger the value of K, the wider will be the operational range. $K = 2$, for example, gives an operational range of $0 < d_a < 0.5$, whereas $K = 6$ widens the range to $0 < d_a < 0.83$. It should be noted that the boundaries given by (26) and (27) represent whether the diode D_a conduct. When the TPC operates near the boundaries, the diode current i_{Da} might be discontinuous in Modes 1 or 2 due to

ripple components originating from inductors and capacitors (see Fig. 6). Hence, the TPC might be unstable near the boundaries of (26) and (27), and it should be designed with considering a margin.

These equations suggest that loads must be properly chosen so that the constraints of (26) and (27) are satisfied at any expected duty cycles. In EPSs of communication satellites and planetary probes, for example, solar energy is always available except for when satellites are in short eclipse periods or special events [26], [27]. Hence, batteries are charged very slowly, and K can be even greater than 6 and 10 for communication satellites [26] and planetary probes [27], respectively.

It is noteworthy that these operation criteria can be easily eliminated by replacing D_a with a switch that allows reverse current flow, and therefore the proposed TPC can operate with an arbitrary value of K without being restricted by the operation constraints discussed above. An additional switch, however, slightly increases the circuit complexity and, therefore, is not recommended if the circuit simplification is prioritized over extending an operation region.

D. Control Scheme

The control block diagram for the proposed PWM-TPC is depicted in Fig. 10. Control blocks are switched by the mode selector depending on operation modes, and V_a and V_b are controlled with separate PI controllers. In the SIDO mode, V_a and V_b are regulated by manipulating d_a and d_b, respectively. In the SISO mode, on the other hand, d_b is manipulated based on the error signal of V_a because the PWM-TPC operates as an ordinary single-input–single-output boost converter, while d_a can be an arbitrary value in the SIDO mode, as discussed in Section IV-B. In the MPPT mode, V_{in} and I_{in} at the input port are controlled by adjusting d_a based on an MPPT algorithm, while the battery port buffers the fluctuating input power so as

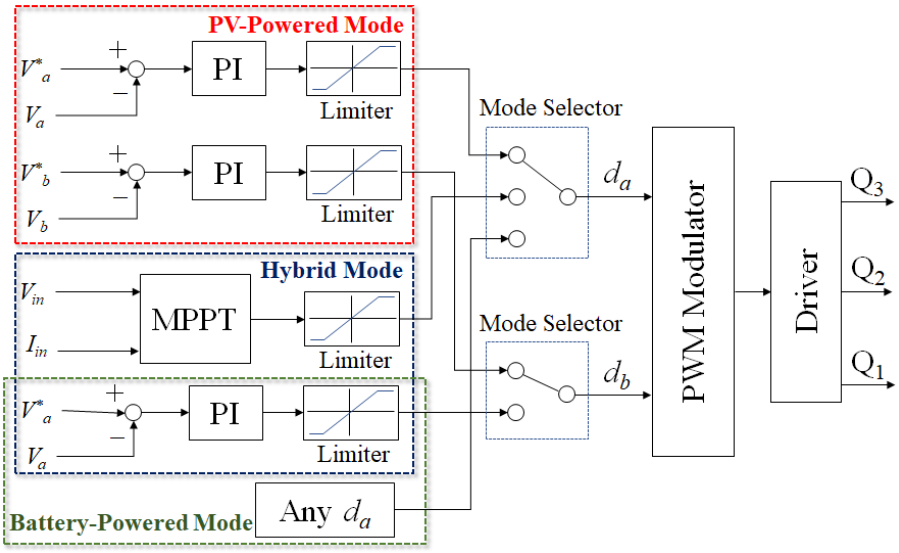


Fig. 10. Control block diagram.

to regulate V_a by manipulating d_b. Any MPPT algorithms can be employed for the proposed PWM-TPC, and a traditional hill climbing-based MPPT will be used for the experimental verification in Section VI-E.

E. Startup Operation

As mentioned in Section III, V_{Ca} under steady-state conditions is $V_{in} - V_a$, and switches can be rated to block only V_a thanks to C_a. At the beginning of a startup, however, C_a is not charged (i.e., $V_{Ca} = 0$), and a full input voltage V_{in} might momentarily be applied to switches. To avoid this situation, Q_r in the startup circuit is turned on to slowly charge C_{in} through R_r. At the same time, gating signals for Q_1–Q_3 are applied so that C_a is also slowly charged. After C_{in} and C_a are charged to V_{in} and $V_{in} - V_a$, respectively, Q is turned on to avoid a steady-state loss in R_r. This simple start-up operation momentarily generates power loss in R_r but would be acceptable in low-power small satellite applications where the simplicity is of great importance.

V. Quantitative Comparison

The quantitative comparison among the proposed PWM-TPC (Fig. 5), a conventional nonisolated TPC [19] [Fig. 11(a)] and a conventional regulated bus system having two separate converters [Fig. 11(b)] are performed from the viewpoints of circuit volume and voltage and current stress in semiconductor devices. Although a PV panel, load, and battery are used as V_{in}, V_a, and V_b, respectively, in Fig. 11(a), this topology is essentially identical to the TPC presented in [19], in which a load, electric double-layer capacitor, and fuel cell are used as V_{in}, V_a, and V_b.

A. Size Metrics

Total energies stored in passive elements are used as circuit volume metrics in this section. The largest values of total stored energies among three operation modes (i.e., the SIDO, SISO, and MPPT modes) were

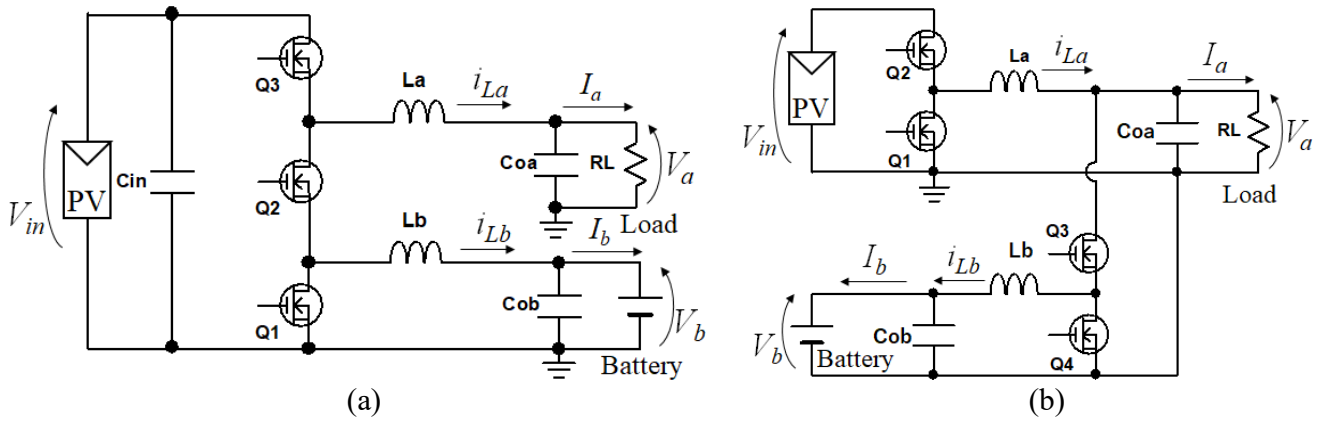


Fig. 11. (a) Conventional nonisolated TPC [19]. (b) Conventional regulated bus system having two separate converters.

used for the comparison as these values vary depending on operation modes. The quantitative comparison was performed with $K = 5.0$ (i.e., the battery power is one-fifth of the load power in the SIDO mode), which corresponded to $M_a < 0.8$ according to (12), (26) and (27). This condition is identical to that of the experiments (see Section VI).

In general, size of passive elements, such as capacitors and inductors, is proportional to its stored energy. In this section, the size metrics S is introduced and defined as the total energies stored in passive elements normalized by the input energy in a single switching cycle, E_{in} (= $V_{in}I_{in}T_S$, where T_S being the switching period);

$$S = \frac{1}{E_{in}}\left(\sum_{Inductors}\frac{\beta E_L}{\alpha_L} + \sum_{Capacitors}\frac{E_C}{\alpha_C}\right) = \frac{1}{E_{in}}\left\{\frac{\beta(E_{La}+E_{Lb})}{\alpha_L} + \frac{E_{Ca}}{\alpha_C}\right\} \tag{28}$$

where E_L and E_C are the charged or discharged energy in inductors and capacitors, respectively, and α_L and α_C are the ripple factors of the inductor current and the capacitor voltage, respectively. β is the energy density ratio of capacitors to inductors.

$$E_{La} = \int_0^{d_aT_s} |v_{La}i_{La}|dt = \int_{d_aT_s}^{T_s} |v_{La}i_{La}|dt \tag{29}$$

$$E_{Lb} = \int_0^{d_bT_s} |v_{Lb}i_{Lb}|dt = \int_{d_bT_s}^{T_s} |v_{Lb}i_{Lb}|dt \tag{30}$$

$$E_{Ca} = V_{Ca}\int_0^{d_aT_s} |i_{Ca}|dt = V_{Ca}\int_{d_aT_s}^{T_s} |i_{Ca}|dt \tag{31}$$

An energy density of discrete capacitors is generally in the range of more than three orders of magnitude greater than that of similarly scaled inductors [28]–[30], meaning β = 100–1000. Typical flux swings of inductors are in the range of 20%–40% (i.e., $0.2 < \alpha_L < 0.4$), while capacitor voltage ripple ratios should be constrained below 10% (i.e., $\alpha_C < 0.1$) [28]. In this section, the quantitative comparison on S was performed with $\alpha_L = 0.3$, $\alpha_C = 0.03$ and $\beta = 100$. The lower the value of S, the smaller will be the circuit volume.

The charged or discharged energies of L_a, L_b and C_a in the proposed PWM-TPC are listed in Table I. In the SIDO mode, Converter A processes the largest power among three operation modes, and therefore, the charged and discharged energies of L_a and C_a also become the largest as they are in Converter A. The energy values of L_b, on the other hand, peaks in the SISO mode, in which Converter B processes the entire load power. Energy values in the MPPT mode are not shown because these are the lowest among the three

Table I. Charged and discharged energies in passive elements in proposed TPC.

Element	SIDO	SISO
L_a	$\frac{6P_a(2M_a-1)(1-M_a)T_s}{5M_a}$	—
L_b	$\frac{P_a(M_a-M_b)T_s}{5M_a}$	$\frac{P_a(M_a-M_b)T_s}{M_a}$
C_a	$\frac{6P_a(1-M_a)^2T_s}{5M_a}$	—

Table II. Charged and discharged energies in passive elements in conventional TPC.

Element	SIDO	SISO
L_a	$P_a(1-M_a)T_s$	$P_a(1-M_a)T_s$
L_b	$\frac{P_a(1-M_b)T_s}{5}$	$P_a(1-M_b)T_s$

Table III. Charged and discharged energies in passive elements in conventional regulated bus system.

Element	SIDO	SISO
L_a	$\frac{6P_a(1-M_a)T_s}{5}$	—
L_b	$\frac{P_a(M_a-M_b)T_s}{5M_a}$	$\frac{P_a(M_a-M_b)T_s}{M_a}$

operation modes. Charged or discharged energies of L_a and L_b in the conventional TPC and conventional regulated bus system were also formulated in Tables II and III, respectively.

The calculated size metrics of the proposed PWM-TPC, conventional nonisolated TPC [19] and conventional regulated bus system are compared in Fig. 12. The comparison was performed with varying d_a and d_b so that the voltage conversion ranges are $0.5 < M_a < 1.0$ and $0 < V_b/V_a < 1.0$. It should be noted that results in Fig. 12 are independent on voltage and current magnitude because the size metrics S is normalized by E_{in} ($= V_{in}I_{in}T_S$). Input and output filter capacitors were excluded from the comparison as their stored energies are nearly identical in all systems. The area enclosed with the solid line in Fig. 12(a) is the allowable operation region of the proposed PWM-TPC. The proposed TPC exhibited the lowest S at any

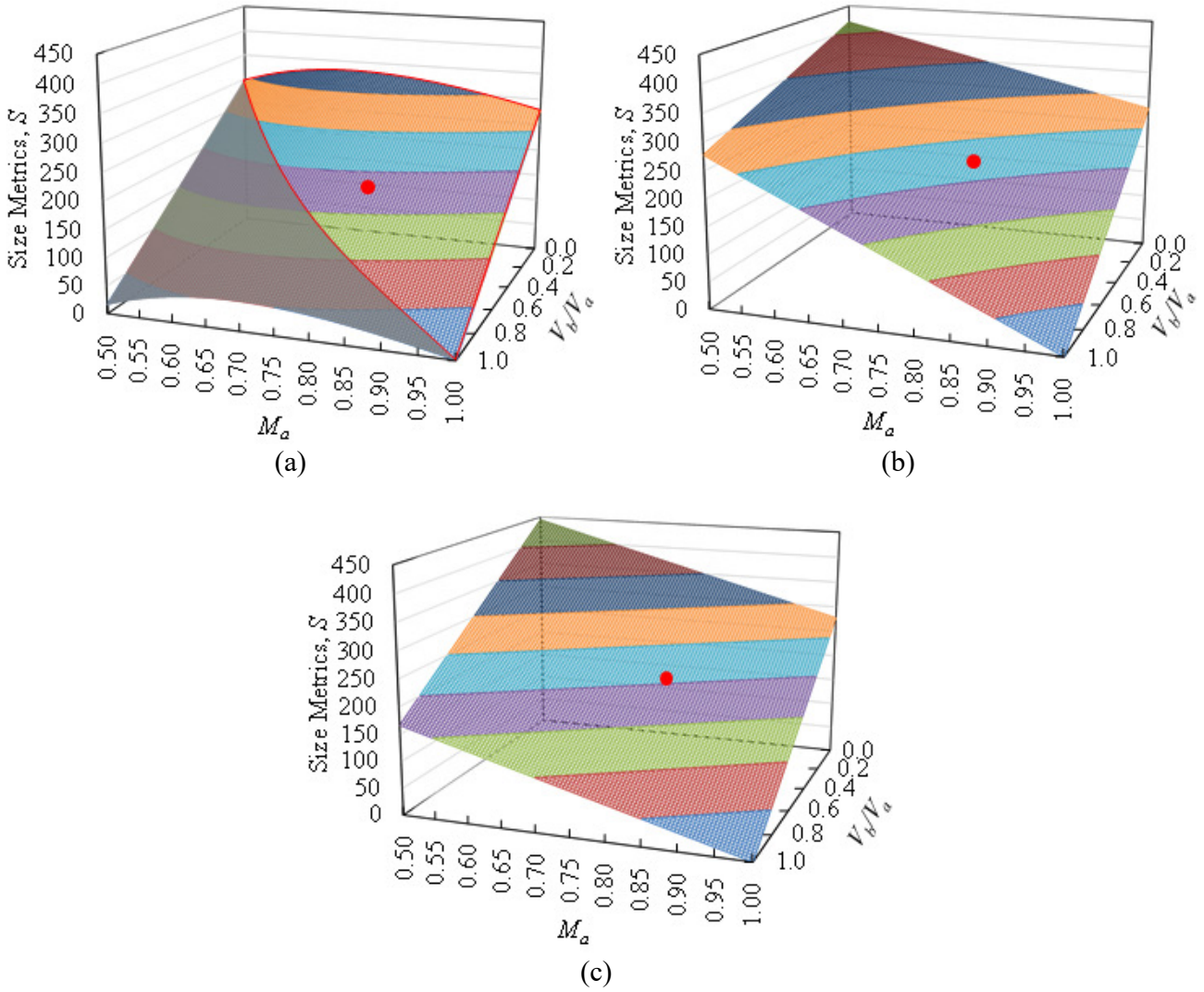


Fig. 12. Comparison on size metrics S among (a) proposed PWM-TPC, (b) conventional nonisolated TPC [19] and (c) conventional regulated bus system.

voltage conversion ratios chiefly because the stored energies in L_a can be reduced thanks to the capacitor C_a whose energy density was 100 times greater than that of inductors (i.e., $\beta = 100$). The difference between the conventional TPC and conventional power system is attributable to the difference in the applied voltage across L_b. The comparative results revealed the proposed PWM-TPC could miniaturize its passive components by 18.4% and 10.9% in comparison with the conventional TPC and regulated bus system, respectively, at the same condition, as indicated with the red points in Fig. 12 (i.e., at $M_a = 0.8$ and $M_b = 0.5$). Hence, the proposed PWM-TPC would achieve reduced circuit volume, though its allowable operation region is narrower—the operation region can be readily extended by replacing D_a with a switch, as discussed in Section IV-C.

B. Total Device Power Rating

Total device power rating (TDPR) that is defined as a sum of voltage-current stresses of all semiconductor devices in a converter is often introduced as an index to quantitatively compare different circuit topologies [31], [32];

Table IV. Voltage and current stresses of semiconductor devices in proposed TPC.

Element	Voltage (V_{max})	Current (I_{max})
Q_1	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$
Q_2	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$
Q_3	$V_a = M_a V_{in}$	$i_{Lb} + i_{Lb} + i_{Da} \approx \frac{P_a}{V_b} + \frac{P_a}{5V_b} + I_{Da} = \frac{P_a}{M_a V_{in}} + \frac{P_a}{5M_b V_{in}} + I_{Da}$
D_a	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$

Table V. Voltage and current stresses of semiconductor devices in conventional TPC.

Element	Voltage (V_{max})	Current (I_{max})
Q_1	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$
Q_2	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$
Q_3	$V_a = M_a V_{in}$	$i_{La} + i_{Lb} \approx \frac{P_a}{V_a} + \frac{P_a}{5V_b} = \frac{P_a}{M_a V_{in}} + \frac{P_a}{5M_b V_{in}}$

Table VI. Voltage and current stresses of semiconductor devices in conventional regulated bus system.

Element	Voltage (V_{max})	Current (I_{max})
Q_1	V_{in}	$i_{La} \approx \frac{6P_a}{5V_a} = \frac{6P_a}{5M_a V_{in}}$
Q_2	V_{in}	$i_{La} \approx \frac{6P_a}{5V_a} = \frac{6P_a}{5M_a V_{in}}$
Q_3	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$
Q_4	$V_a = M_a V_{in}$	$i_{Lb} \approx \frac{P_a}{V_b} = \frac{P_a}{M_b V_{in}}$

$$TDPR = \sum_{Switches\ and\ Diode} \frac{V_{max} I_{max}}{P_{in}} \tag{32}$$

where V_{max} and I_{max} are the maximum voltage and current stresses, respectively. The lower the value of TDPR, the less amount of silicon will be necessary at a given power rating of a converter.

V_{max} and I_{max} of each semiconductor device in the proposed TPC are listed in Table IV, in which values of I_{max} are approximated using average values. All the voltage stresses are equal to V_a. Q_1, Q_2, and D_a are exposed to the largest current stress in the SISO operation mode as Converter B processes the whole power, as can be seen in Fig. 9. The current stress of Q_3, on the other hand, becomes the highest in the SIDO operation mode as all currents flow through it [see Fig. 7(a)]. V_{max} and I_{max} of the conventional TPC and conventional system are also formulated and are shown in Tables V and VI, respectively.

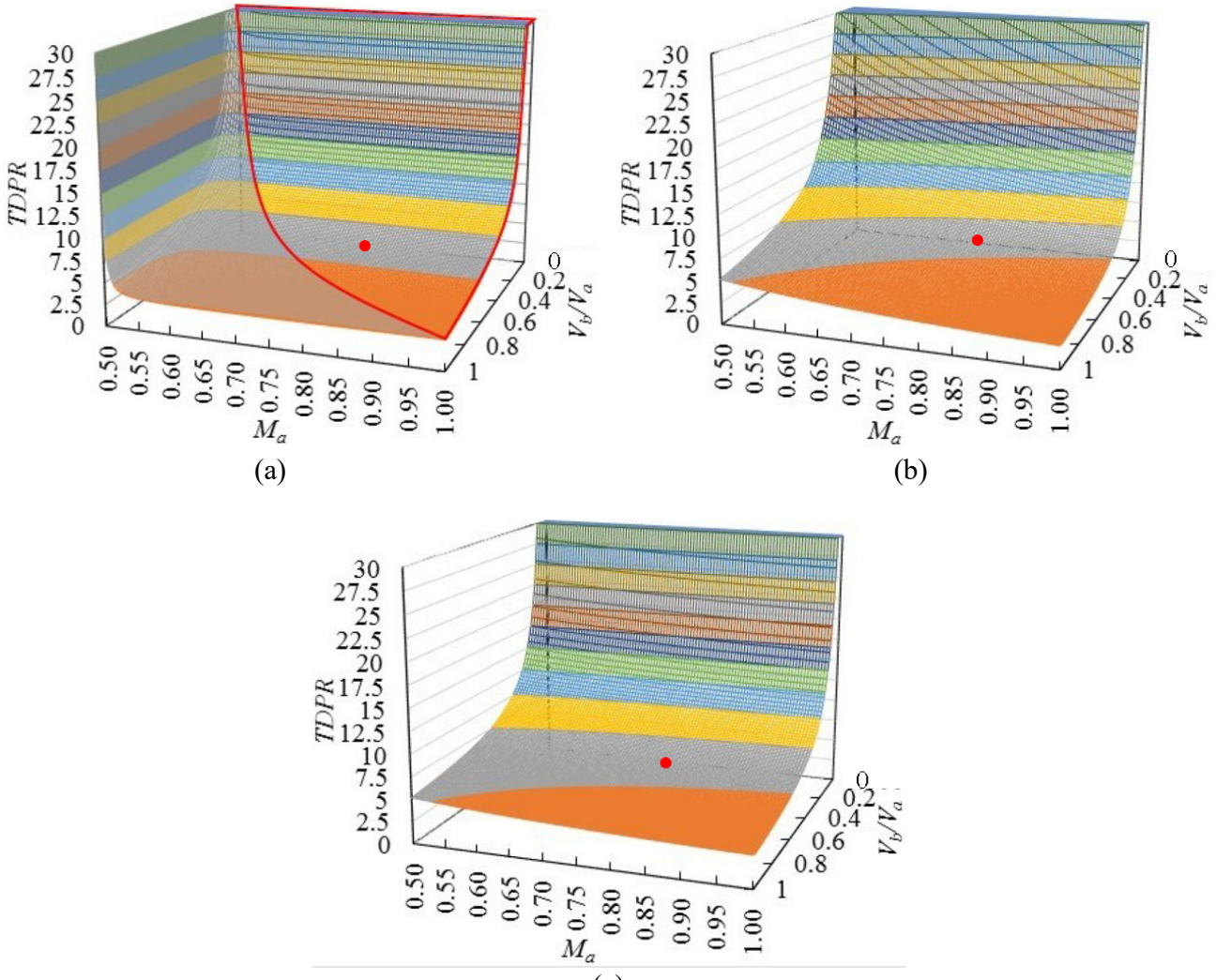


Fig. 13. Comparison on TDPR among (a) proposed PWM-TPC, (b) conventional nonisolated TPC [19] and (c) conventional regulated bus system.

The calculated TDPRs of the proposed TPC, conventional TPC, and conventional regulated bys system are shown and compared in Fig. 13. The area enclosed with the solid line in Fig. 13(a) is the allowable operation area of the proposed TPC with K = 5.0. TDPR of the proposed TPC increased as M_a neared 0.5 because M_a = 0.5 corresponded to an extreme duty cycle operation according to (23). As M_a moved away from 0.5, the proposed TPC exhibited lower TDPR than did the conventional system. The lower TDPR characteristics were chiefly because of the reduced voltage stress of switches Q_1–Q_3 and D_a thanks to C_a, which is connected in series with Q_1–Q_3. Switches in the conventional system, on the other hand, are rated for the full input voltage, hence resulting in larger TDPR.

Although the operation area of the proposed TPC is narrower due to the operational constraints and limited voltage conversion range as discussed in Section IV-C, the reduced size and lower TDPR would be an appealing feature compared to the conventional TPC and conventional regulated bus system.

VI. Experimental Results

A. Prototype

A 240-W prototype of the proposed nonisolated PWM-TPC with K = 5.0 at a full load (P_a = 200 W and P_b = 40 W) was designed for V_{in} = 60 V, V_a = 48 V and V_b = 24 V at a switching frequency f_s = 100 kHz. Applying d_a [see (12)], α_L = 0.3, and α_C = 0.1 into (14) and (16) yields the values of L_a and C_a, as

$$L_a = \frac{(48V - 12V) \times (1 - 0.75) \times 10\mu s}{0.3 \times 4.0\ A} = 75\ \mu\text{H} \rightarrow 100\ \mu H \tag{33}$$

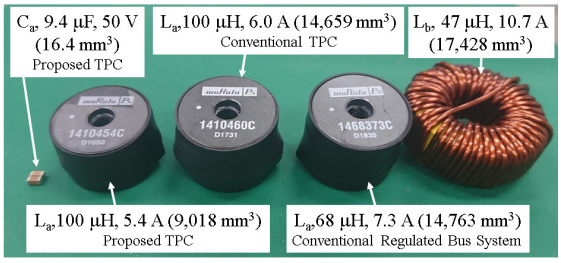


Fig. 14. Actual L_a, L_b, and C_a used for proposed TPC, conventional TPC, and conventional regulated bus system.

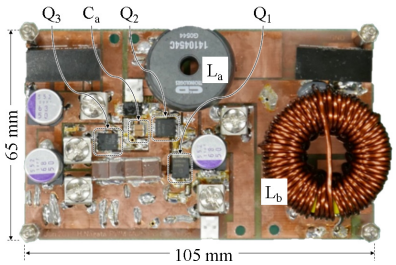


Fig. 15. Photograph of 240-W prototype.

Table VII. Circuit element list.

Symbol	Part Number and Manufacture	Value
L_a	1410454C, Murata	100 µH,
L_b	2309-H-RC, Bourns	47 µH,
C_{in}	CGA9N3X7S2A106K239KB, TDK	Ceramic Capacitor, 10 µF×17
C_a	UMK316AB7475KL, Taiyo Yuden	Ceramic Capacitor, 4.7 µF×2
C_{oa}	50SVPF68M, Panasonic	OS-CON, 68 µF×6
C_{ob}	50SVPF68M, Panasonic	OS-CON, 68 µF×3
D_a	PDS4150, Diodes Zetex	Schottky Diode, V_F = 0.76 V
Q_1– Q_3	BSC360N15NS3, Infineon	R_{on} = 36 mΩ, V_{DS} = 150 V

$$C_a = \frac{4.0\ \text{A} \times (1 - 0.75) \times 10\mu s}{0.1 \times (60\ \text{V} - 48\ \text{V})} = 8.33\ \mu F \rightarrow 9.4\ \mu F \tag{34}$$

Since L_b processes larger current in the SIDO mode, its inductance was determined from (20) by applying d_b [see (19)] and α_L = 0.3, as

$$L_b = \frac{24\ V \times (1 - 0.5) \times 10\mu s}{0.3 \times 8.33\ A} = 48\ \mu H \rightarrow 47\ \mu H \tag{35}$$

The actual L_a, L_b, and C_a used for the prototype of the proposed TPC are compared to those of the conventional TPC and conventional regulated bus systems, as shown in Fig. 14. L_a and L_b were selected so that their maximum current rating was approximately 1.2 times higher than their peak currents. C_a was very tiny compared to L_a and L_b. The total volume of L_a, L_b, and C_a in the proposed TPC was 26,462 mm^3 and was approximately 18% smaller than that of the conventional TPC (32,087 mm^3) and the conventional regulated bus system (32,191 mm^3).

The prototype and its circuit element values are shown in Fig. 15 and Table VII, respectively. In general, a capacitance of class II ceramic capacitors, which are typically used in switching converters due to their high volumetric efficiency, is dependent on a dc bias voltage. Ceramic capacitors for the prototype were selected with considering their dc bias characteristics, similarly to those in typical switching converters.

B. Power Conversion Efficiency in SIDO Mode

The measured key operation waveforms in the SIDO mode at the output power P_a = 200 W and the battery charging power P_b = 20 W are shown in Fig. 16. Spikes found in i_{Lb} were considered due to EMI noise emitted by the inductor L_a using a non-toroidal core. These waveforms agreed well with the theoretical ones shown in Fig. 6, validating the fundamental operation discussed in Section III-A.

The power conversion efficiencies in the SIDO mode, which are defined as

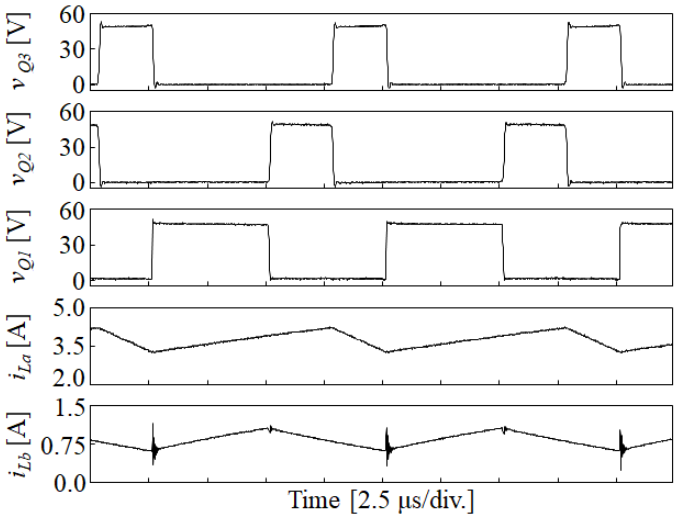


Fig. 16. Measured key operation waveforms in SIDO mode at P_a = 200 W and P_b = 20 W.

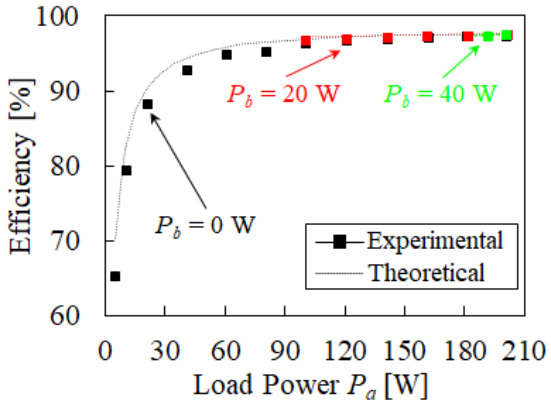
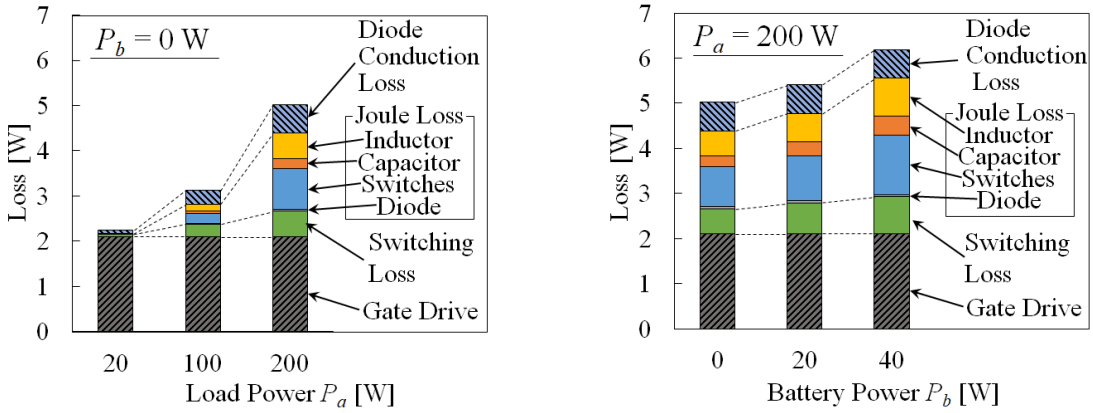


Fig. 17. Measured power conversion efficiencies in SIDO mode.

$$\eta_{SIDO} = \frac{P_a + P_b}{P_{in}} \tag{36}$$

where P_a, P_b, and P_{in} are the load power, battery charging power and input power, respectively. The measured power conversion efficiencies in the SIDO mode at V_a = 48 V, V_b = 24 V and P_b = 0–40 W are shown in Fig. 17. The efficiencies declined in the light-load region because a fixed loss due to gate driving dominated. The measured efficiency at the full load of P_a = 200 W and P_b = 40 W was as high as 97.3%.

The theoretical power conversion efficiency model was established based on the detailed analysis (the model is not shown) and is compared with the measured efficiencies, as depicted with dashed lines in Fig. 17. The theoretical efficiency model agreed satisfactorily with the experimental results. The theoretical loss breakdowns at P_b = 0 W and P_a = 200 W are shown in Figs. 18(a) and (b), respectively. The loss associated with the gate driving was the most dominant factor at any power level. The Joule losses consistently increased with P_a, as shown in Fig. 18(a), and became comparable to the gate driving loss at P_a = 200 W,



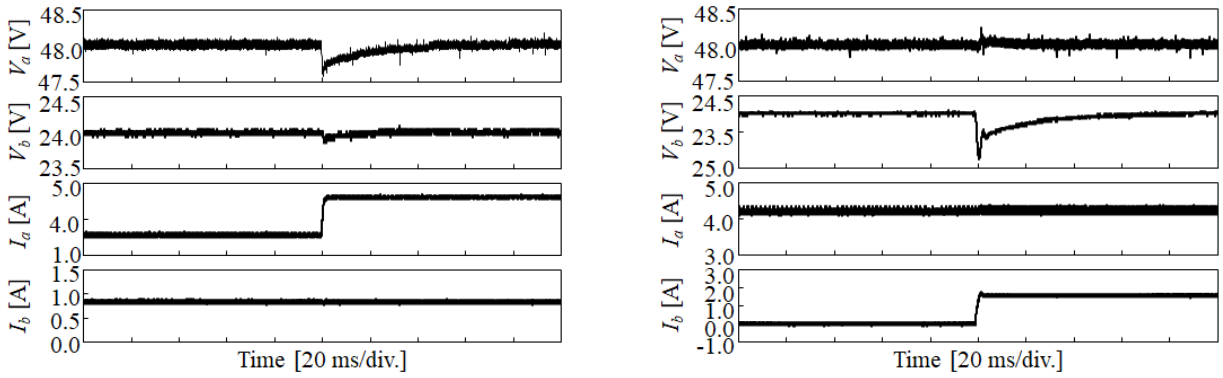
(a) (b)

Fig. 18. Theoretical loss breakdowns in SIDO mode at (a) fixed P_b = 0 W and (b) fixed P_a = 200 W.

at which the highest efficiency was observed. Meanwhile, losses were relatively insensitive to P_b, as shown in Fig. 18(b), chiefly because the power processed by Converter B (P_b < 40 W) was rather smaller than that of Converter A (P_a = 200 W).

C. Transient Response in SIDO Mode

To investigate response characteristics as well as the interdependence between control loops for V_a and V_b, transient responses to the step changes in I_a and I_b were measured, as shown in Fig. 19. The step change in the output current I_a triggered not only an abrupt drop in the output voltage V_a but also a small dip in the battery voltage V_b, as shown in Fig. 19(a), because V_b was theoretically dependent on not only d_b but also d_a, as (13) indicates. Similarly, V_b abruptly dropped in response to the step increase in I_b, as shown in Fig. 19(b). Although V_a was theoretically independent on d_b, V_a rose slightly in response to the step change in I_b. This interdependence was considered due to parasitic elements, including ESRs and stray inductances of Q_3 and C_a, through which currents contributing to not only I_a but also I_b flew, as can be seen in Fig. 7(a).



(a) (b)

Fig. 19. Measured transient responses to step change in (a) load current I_a and (b) battery current I_b in SIDO mode.

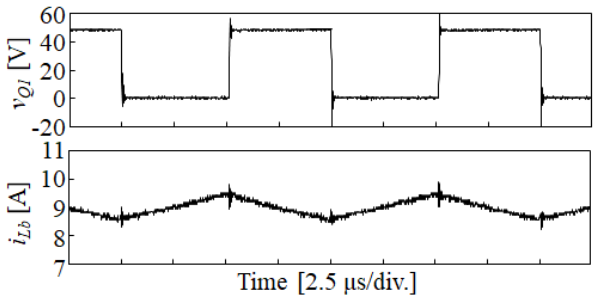


Fig. 20. Measured key operation waveforms in SISO mode.

However, the observed interdependence was very trivial and considered not detrimental. The interdependence would be further mitigated or even eliminated by introducing a decoupling network that can be derived from state-space modeling [8], [23], which will be a part of our future works.

D. Power Conversion Efficiency in SISO and MPPT Modes

The measured key waveforms in the SISO mode at a full load of P_a = 200 W are shown in Fig. 20. d_a was fixed to be 0.75. These waveforms agreed well with the theoretical ones shown in Fig. 8.

The power conversion efficiencies in the SISO or MPPT mode is defined as

$$\eta_{SISO-MPPT} = \frac{P_a}{P_{in} + P_b} \tag{37}$$

It should be noted that, in the case of P_{in} = 0, the converter operates in the SISO mode because of no power available at the input port.

Measured power conversion efficiencies in the SISO and MPPT modes at V_a = 48 V, V_b = 24 V, V_{in} = 60 V and P_{in} = 0–150 W are shown in Fig. 21. The measured efficiency at the full load of 200 W in the SISO mode (i.e., P_{in} = 0 W) was as high as 94.7%. Efficiencies consistently increased with P_{in} in the MPPT mode (i.e., when $P_{in} \neq 0$ W) because of the power-sharing between Converters A and B. At the full load of P_a =

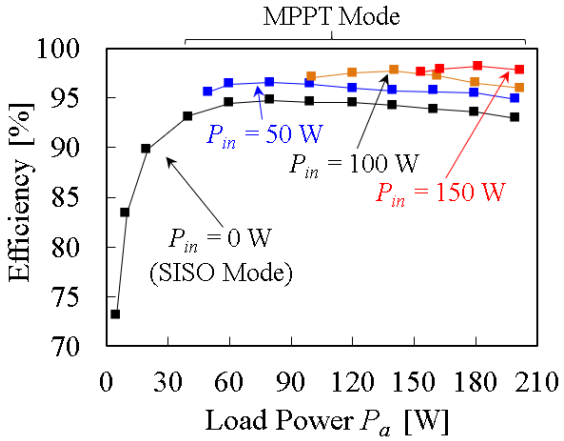


Fig. 21. Measured power conversion efficiencies in SISO and MPPT modes.

200 W in the MPPT mode, for example, P_{in} was 150 W (see the annotation in Fig. 21), and P_b was estimated to be about 50 W. In other words, both Converters A and B shared the total load power of P_a, therefore mitigating RMS currents as well as associated Joule losses in the circuit. In the SISO mode of P_{in} = 0 W, on the other hand, the whole power was processed by Converter B alone, resulting in increased RMS currents and decreased efficiency due to the current concentration to Converter B.

E. Transient Response in MPPT Mode

To verify the control scheme presented in Section III-D, transient responses to the step change in the load power P_a in the MPPT mode were measured. The perturb & observation (P&O)-based hill climbing MPPT algorithm with a sampling interval of 2.0 s and 1%-duty cycle perturbation was employed in this test. A solar array simulator (E4361A, Keysight Technologies) was used as the input power source emulating a PV array characteristic, and its maximum power was set to be 128 W at V_{in} = 60 V and I_{in} = 2.14 A. Meanwhile, V_a was regulated to be 48 V, and the load power P_a was step-increased from 100 to 200 W. Instead of an actual battery, a bidirectional power supply with V_b = 24 V was used to emulate bidirectional power flow at the battery port.

The measured transient responses are shown in Fig. 22. Before applying the step change, I_b was positive, meaning the battery port was being charged with the surplus power. As I_a (or P_a) increased, I_b quickly became negative, and the battery port started discharging to complement the deficit power. Although slightly influenced, V_{in} and I_{in} nearly unchanged before and after the step change, thanks to the MPPT control. V_a was also regulated to be 48 V by the output voltage control loop manipulating d_b (see Fig. 10).

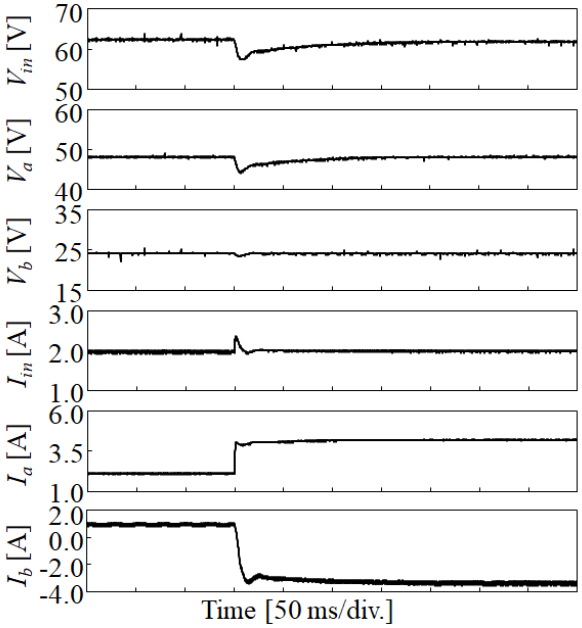


Fig. 22. Measured transient responses in MPPT mode.

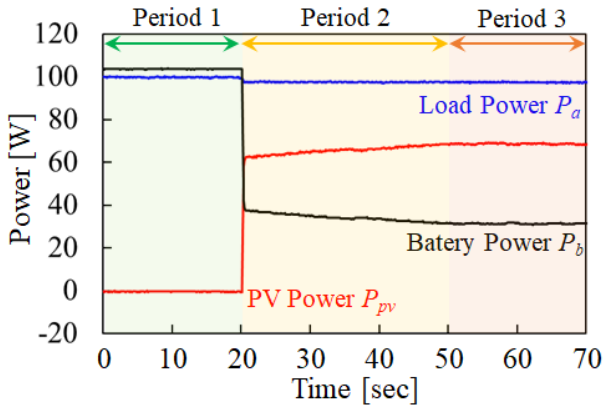


Fig. 23. Experimental results of power balancing test employing MPPT control.

In summary, the results demonstrated that the battery port responded to the load change while the PV array kept generating its maximum power.

Transient characteristics under a change in the maximum input power were also measured emulating irradiance change. For the fixed load power P_a = 100 W, the maximum power of the PV array was changed from 0 to 70 W so that the operation changed from the SISO to MPPT modes.

The measured response characteristics are shown in Fig. 23. In Period 1, the PV array was not available (i.e., P_{in} = 0 W), and hence the battery alone supplied the entire load power of 100 W. This period corresponded to the SISO mode. In Period 2, the maximum power of the PV array was abruptly increased to 70 W, and consequently the battery together with the PV array started supplying power to the load. The extracted power from the PV array gradually increased as the PWM-TPC operated in search for the MPP in Period 2. In Period 3, the PWM-TPC finally came to the operation at the MPP. The maximum power of 70 W was extracted from the PV array, while the deficit power of 30 W was supplied from the battery.

VII. Conclusions

The simple nonisolated PWM-TPC has been proposed in this paper to address the issues of the conventional nonisolated TPCs. Two different PWM converters are integrated into a single unit with sharing switches, hence simplifying the system and reducing the circuit complexity. In addition, the proposed PWM-TPC offers the major advantages of the reduced voltage rating of switches and miniaturized inductors, thanks to the capacitor C_a inserted in series with switches.

Based on the operation analysis, the voltage conversion ratios and the operation constraints have been mathematically determined. The quantitative comparison for the proposed PWM-TPC, conventional nonisolated TPC, and the conventional regulated bus system having two separate PWM converters was

performed from the viewpoints of circuit volume. The comparative results revealed the volume of the passive components in the proposed PWM-TPC could be miniaturized by approximately 19% in comparison with the conventional nonisolated TPC.

The experimental verification tests were performed using the 240-W prototype. The measured efficiency at the full load of 240 W in the SIDO mode was as high as 97.3%. The measured transient response characteristics demonstrated that the load and battery voltages could be independently regulated with minor interdependence. The transient characteristics in the MPPT mode were also measured, and the result demonstrated the maximum power from the PV array could be extracted while the deficit power was supplied from the battery by the proposed PWM-TPC.

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Hikaru Nagata was born in 1994. He received the B.E. and M.S. degrees in electrical and electronics engineering from Ibaraki University, Ibaraki, Japan in 2016 and 2018, respectively. He is currently with Hitachi Ltd. His research interests include dc-dc converters for photovoltaic and energy storage systems.

Masatoshi Uno (M'06) was born in Japan in 1979. He received the B.E. degree in electronics engineering and the M.E. degree in electrical engineering from Doshisha University, Kyoto, Japan, and the Ph.D. degree in space and astronautical science from the Graduate University for Advanced Studies, Hayama, Japan, in 2002, 2004, and 2012, respectively.

In 2004, he joined the Japan Aerospace Exploration Agency, Sagamihara, Japan, where he developed spacecraft power systems including battery, photovoltaic, and fuel cell systems. In 2014, he joined the Department of Electrical and Electronics Engineering, Ibaraki University, Ibaraki, Japan, where he is currently an Associate Professor of Electrical Engineering.

His research interests include switching power converters for renewable energy systems, life evaluation for EDLCs and lithium-ion batteries, and development of spacecraft power systems. Dr. Uno received the Isao Takahashi Power Electronics Award in 2018.

Figure Captions

Fig. 1. Schematic diagrams of (a) unregulated bus system, (b) regulated bus system, and (c) regulated bus system with TPC.

Fig. 2. PWM converters for the proposed TPC: (a) Unidirectional step-down converter (Converter A), (b) bidirectional converter (Converter B).

Fig. 3. Key operation waveforms of unidirectional step-down PWM converter.

Fig. 4. Operation mode of unidirectional step-down PWM converter: (a) Mode 1, (b) Mode 2.

Fig. 5. Proposed nonisolated PWM-TPC.

Fig. 6. Key operation waveforms in SIDO mode.

Fig. 7. Current flows in SIDO mode: (a) Mode 1, (b) Mode 2, (c) Mode 3.

Fig. 8. Key operation waveforms in SISO mode.

Fig. 9. Current flows in SISO mode: (a) Mode 1, (b) Mode 2.

Fig. 10. Control block diagram.

Fig. 11. (a) Conventional nonisolated TPC [19]. (b) Conventional regulated bus system having two separate converters.

Fig. 12. Comparison on size metrics S among (a) proposed PWM-TPC, (b) conventional nonisolated TPC [19] and (c) conventional regulated bus system.

Fig. 13. Comparison on TDPR among (a) proposed PWM-TPC, (b) conventional nonisolated TPC [19] and (c) conventional regulated bus system.

Fig. 14. Actual L_a, L_b, and C_a used for proposed TPC, conventional TPC, and conventional regulated bus system.

Fig. 15. Photograph of 240-W prototype.

Fig. 16. Measured key operation waveforms in SIDO mode at P_a = 200 W and P_b = 20 W.

Fig. 17. Measured power conversion efficiencies in SIDO mode.

Fig. 18. Theoretical loss breakdowns in SIDO mode at (a) fixed P_b = 0 W and (b) fixed P_a = 200 W.

Fig. 19. Measured transient responses to step change in (a) load current I_a and (b) battery current I_b in SIDO mode.

Fig. 20. Measured key operation waveforms in SISO mode.

Fig. 21. Measured power conversion efficiencies in SISO and MPPT modes.

Fig. 22. Measured transient responses in MPPT mode.

Fig. 23. Experimental results of power balancing test employing MPPT control.